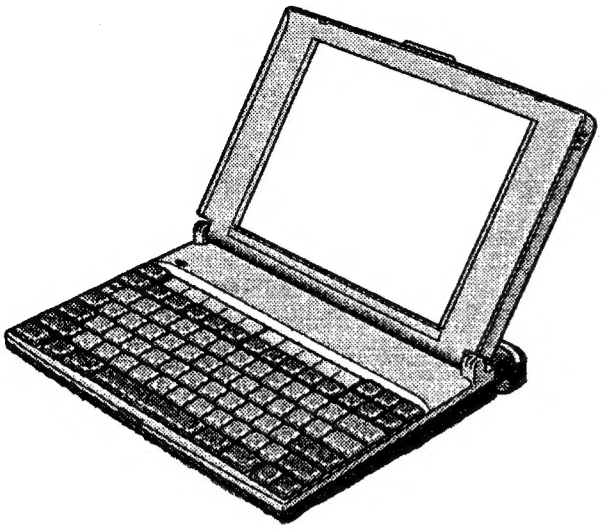
SHARP SERVICE MANUAL

CODE: 00ZPV5000SP/E



Handheld PC Pro

PV-5000
MODEL PV-5000A

CONTENTS

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

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The contents are subject to change without notice.

CHAPTER 1. SPECIFICATIONS

The PV-5000 use the Microsoft® Windows® CE operating system, which is similar to the Microsoft Windows 95/98 and Window NT 4.0 operating systems.

The Microsoft Windows® CE operating system comes standard with the following programs:

- Microsoft Pocket Word
- Microsoft Pocket Excel
- Microsoft Pocket PowerPoint
- Windows CE Services
- Pocket Internet Explorer
- Pocket Outlook™ (Contacts/Calendar/Tasks/Inbox)
- Microsoft Pocket Access
- Active Sync
- Microsoft Ink Writer

etc

Additional programs from SHARP in this device make your mobile life even more comfortable:

- PC File viewer (to view desktop PC files)
- MPEG Player (to play MPEG movies)
- Image Editor (to edit images)

DISPLAY SECTION

DISPLAY:	8.2", 4096 color, high-contrast LCD touch screen with backlight, 640 × 480 (VGA)

POWER SUPPLY

Main: (built-in)	10.8V, Lithium-ion Rechargeable Battery Pack, 22VDC, AC adaptor
Backup:	3V DC, CR2032 lithium battery

POWER CONSUMPTION

5 W (using built-in main battery)

18.6 W (using AC adaptor)

DIMENSIONS

237 (W) × 195 (D) × [Front] 28.2 (H) mm [Rear] 37.4 (H) mm

(9-11/32) (W) × 7-11/16 (D) × [Front]1-1/8 (H) mm [Rear] 1-15/32 (H) mm)

Weight

Approx. 1.22 kg (2.7 lb)

Interfaces

Serial port

RJ-11 phone jack (with internal modem model only)

Infrared port (IrDA compliant)

PC Card slot: 1 (Type II)

Audio: Speaker

Internal Fax/Modem (may not be arailable in same countries)

Transmission speed:	Data modem 33.6 kbps, Fax modem 14.4 kbps

* Compliant only with North American standards

Memory

16 MB or 32 MB (according to model)

Battery life (built-in main battery)

- Approx. 10 hour with continuous display and dimmed backlight (without using the internal fax/modem), at ambient temperature o 25°C (77°F)
- Approx. 8 hours with 5 minutes operation alternating with 55 minutes of display only at medium backlight brightness, at ambient temperature of 25°C (77°F)
- Approx. 4.5 hours with continuous internet access using the internal fax/modem at maximum backlight brightness, at ambient temperature of 25°C (77°F)
- Approx. 2 hours with continuous monitoring of a subject at maximum backlight brightness using the operational digital camera card CE-AG04, at ambient temperature of 25°C (77°F)
- Battery life may vary depending on usage.

Memory backup time

Approx. 5 days (with depleted main battery and new CR-2032 backup battery)

- Memory backup time may vary depending on the condition of the main battery and the backup battery.
- Please charge the main battery promptly after the charge becomes low. Leaving it uncharged for an extended period of time will result in rapid depletion of the backup battery, and possible loss of all data.

Battery charging time

Approx. 2 hours and 30 minutes

Operating temperature: 0° to 40°C (32° to 104°F)

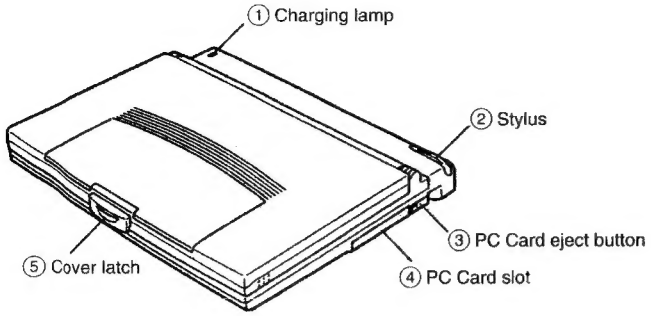
Accessories

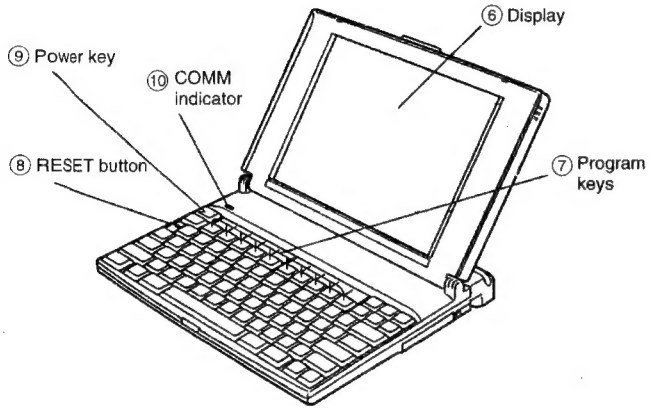
Serial cable, Modular phone cable (with internal modem model only), CD-ROM from Microsoft, CD-ROM from SHARP, AC adaptor (EA-J01V), AC power cord, Screw driver, two spare screws, Operation Manual, CR2032 lithium backup.

Accessories (optional)

Color Digital camera card CE-AG04.

Part names and functions





① Charging lamp

Flashes while the built-in main battery is charging, lights steadily when the battery is fully charged.

② Stylus

Use it to write on the display or navigate through the software.

③ PC Card eject button

Swing out and push to eject the inserted PC Card.

④ PC Card slot

For inserting a Type II PCMCIA card. A protection Card is inserted at the factory for protection.

⑤ Cover latch

Press to open the device.

⑥ Display

Shows information and also functions as a "touch screen" for selecting operations, data entry, etc.

⑦ Program keys

Press to start the indicated program.

⑧ RESET button

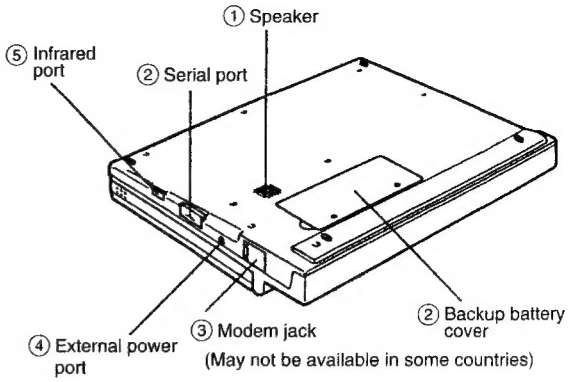
Press to reset and initialize the device.

⑨ Power key

Press to turn on the device. Press for one second to turn off the device.

⑩ COMM

Lights during communication through the internal fax/modem interface, the infrared port, or the serial port.



① Speaker

② Backup battery cover

Open to replace the backup battery or perform a full reset, as necessary.

③ Modem jack (May not be available in some countries.)

For fax and data communication. Compliant only with North American standards.

④ External power port

For connecting to the AC adaptor included in the package.

⑤ Infrared port

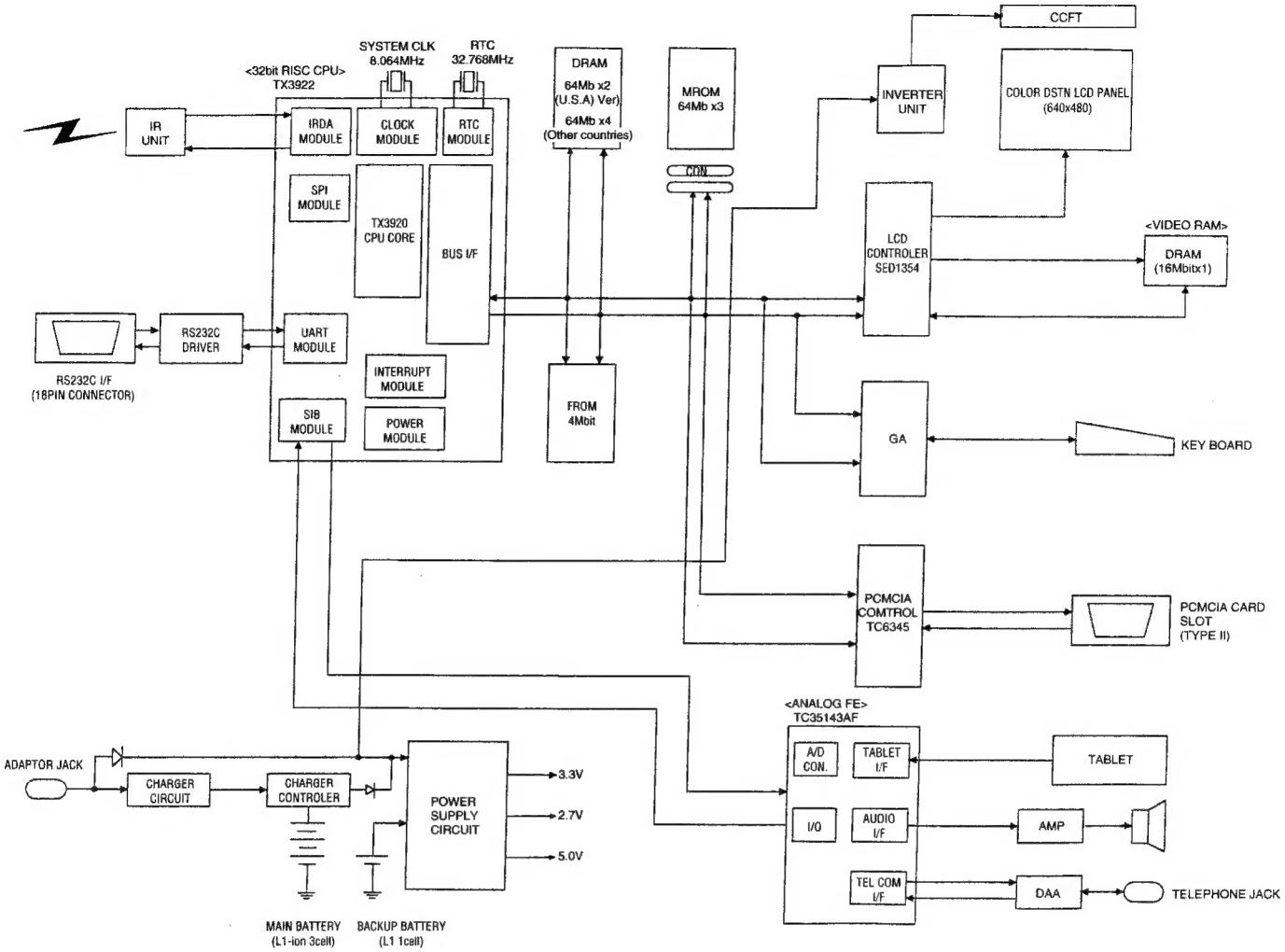
For wireless communication with other handheld PCs, infrared-capable notebook and desktop PCs, and printing to infrared-capable printers.

⑥ Serial port

For connecting to a desktop PC for data transfer or to a printer for printing.

CHAPTER 2. HARDWARE DESCRIPTION

1. BLOCK DIAGRAM



2. DESCRIPTION OF LSI

2-1. CPU (TMPR3922U)

1) GENERAL DESCRIPTION

The TMPR3922U is a single-clip integrated digital ASSP for PDA (Personal Digital Assistants). The TMPR3922U consists of PDA system support logic, integrated with the TX3920 processor Core designed by Toshiba.

2) FEATURES

■ **R3000A-based TX3920 Processor Core**

RISC architecture developed by MIPS Group, a division of silicon Graphics, Inc.

Toshiba has added its own multiply-add and branch-likely instructions.

A single-cycle multiply/accumulate module to allow integrated DSP functions, such as a software modem for high-performances standard data and fax protocols

Instruction cache: 16K bytes (2 Way); data cache: 8K bytes (2 Way)

On-chip Translation Lookaside Buffer (TLB) with 64 × 64-bit wide entries, each of which maps 4K/16K/64K/256K/1M/4MByte page

■ **Built-in peripheral circuit**

Clock generator with built-in sixteenfold-frequency phase-locked loop (PLL)

Four-stage write buffer

A high performance and flexible Bus Interface Unit

Multiple DMA channels

Memory controller for DRAM (EDO), SDRAM, SRAM, ROM, Flash Memory and PCMCLA

Power management unit

Big/Little endian

■ **Low power dissipation**

3.3V (I/O)/2.7V (Internal) operation

Standby Current 10μA (typ)

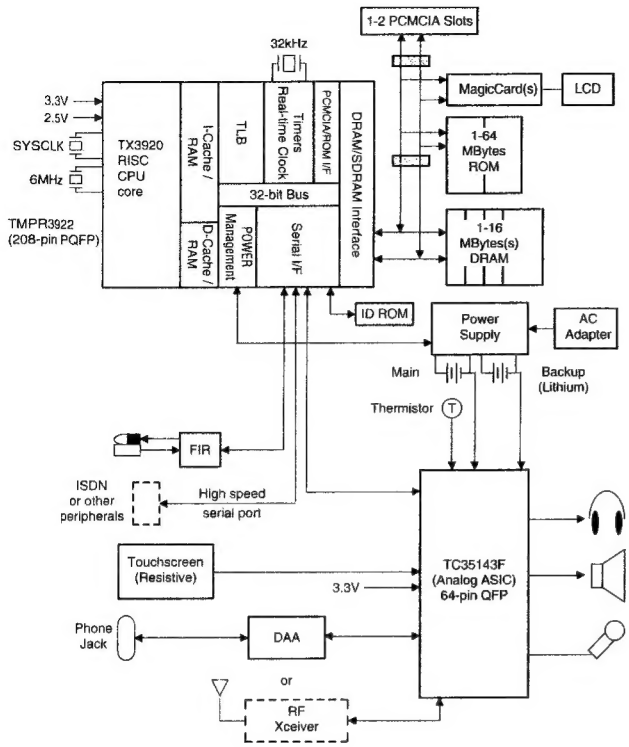
CPU clock stop mode

Power down modes for individual internal peripheral modules

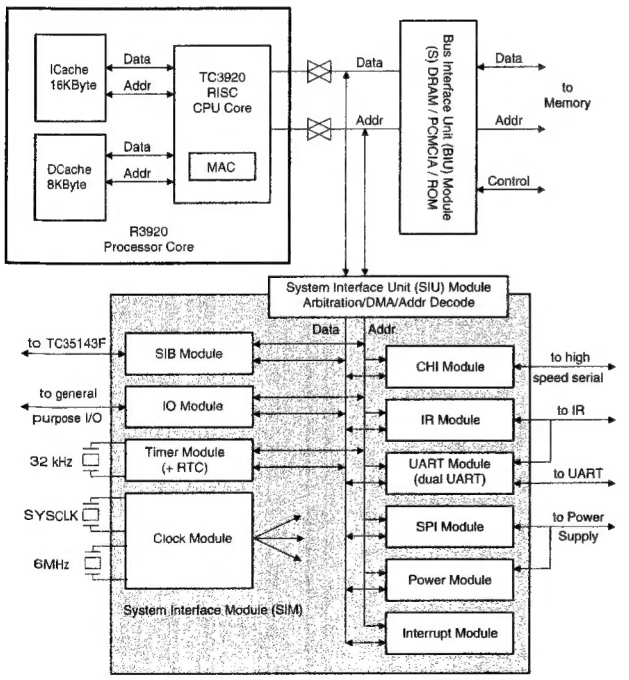
■ **Plastic LQFP 208-pin package**

3) SYSTEM CONFIGURATION

3.1 SYSTEM BLOCK DIAGRAM



3.2 TMPR3922 DIAGRAM



4) PINS

4.1 PIN ASSIGNMENT

NO.	I/O	SIGNAL NAME
1	—	VDDH
2	I/O	D[0] (D[24])
3	—	VSS
4	I/O	D[1] (D[25])
5	I/O	D[2] (D[26])
6	—	VDDL
7	I/O	D[3] (D[27])
8	—	VSS
9	I/O	D[4] (D[28])
10	—	VDDLS
11	I/O	D[5] (D[29])
12	I/O	D[6[(D[30])
13	—	VSS
14	I/O	D[7] (D[31])
15	—	VSS
16	I/O	D[8] (D[16])
17	—	VDDH
18	I/O	D[9] (D[17])
19	I/O	D[10] (D[18])
20	—	VSS
21	I/O	D[11] (D[19])
22	—	VDDH
23	I/O	D[12] (D[20])
24	I/O	D[13] (D[21])
25	—	VSS
26	I/O	D[14] (D[22])
27	I/O	D[15] (D[23])
28	—	VDDL
29	I	ENDIAN
30	NC	RESERVED
31	NC	RESERVED
32	NC	RESERVED
33	—	VSS
34	NC	RESERVED
35	I/O	IO[12]
36	—	VDDLS
37	O	SIBMCLK
38	—	VSS
39	O	SIBSCLK
40	O	SIBSYNC
41	I	SIBDIN
42	O	SIBDOUT
43	—	VDDH
44	I	SIBIRQ
45	I/O	I/O[13]
46	I/O	IO[14]
47	I/O	IO[15]
48	—	VSS
49	I/O	CHICLK
50	I/O	CHIFS
51	I	CHIDIN
52	O	CHIDOUT

NO.	I/O	SIGNAL NAME
53	—	VDDH
54	I	RXD
55	O	TXD
56	I	IRINA
57	I	IRINB
58	O	FIROUT
59	O	IROUT
60	—	VSS
61	—	VDDH
62	I	CARDET
63	O	RXPWR
64	I/O	IO[3]
65	I/O	IO[2]
66	—	VSS
67	O	SPICLK
68	I	SPIIN
69	O	SPIOUT
70	—	VDDLS
71	I	TESTCPU
72	I	TESTIN
73	O	BCLK
74	I	TESTAIU
75	—	VSS
76	I	VCC3
77	O	BC32K
78	—	VDDL
79	I	C32KIN
80	O	C32KOUT
81	—	VSS
82	O	PWRCS
83	I	PWRINT
84	I	PWROK
85	I/O	IO[8]
86	I	ONBUTN
87	I	PON*
88	I	CPURES*
89	—	VDDL
90	I	C6MIN
91	O	C6MOUT
92	—	VSS
93	I/O	IO[9]
94	I/O	IO[10]
95	I/O	IO[11]
96	—	VSSP[PLL]
97	—	VDDP[PLL]
98	O	C48MOUT
99	I/O	IO[7]
100	I/O	IO[6]
101	I/O	IO[5]
102	—	VSSP[PLL]
103	I/O	IO[1]
104	—	VDDP[PLL]

NO.	I/O	SIGNAL NAME
105	I	CARD2WAIT*
106	O	CARD2CSH*
107	O	CARD2CSL*
108	I/O	IO[0]
109	—	VSS
110	O	CARDIORD*
111	O	CARDIOWR*
112	O	CARDREG*
113	I	CARD1WAIT*
114	—	VDDH
115	O	CARDDIR*
116	—	VDDLS
117	O	CARD1CSL*
118	O	CARD1CSH*
119	—	VSS
120	I	MCS1WAIT*
121	I	MCS0WAIT*
122	O	MCS1*
123	O	MCS0*
124	O	CS3*
125	O	CS2*
126	O	CS1*
127	—	VDDL
128	I	SYSCLKIN
129	O	SYSCLKOUT
130	—	VSS
131	—	VSS
132	—	VDDLS
133	I/O	D[31] (D[7])
134	I/O	D[30] (D[6])
135	—	VSS
136	I/O	D[29] (D[5])
137	—	VDDH
138	I/O	D[28] (D[4])
139	I/O	D[27] (D[3])
140	—	VSS
141	I/O	D[26] (D[2])
142	—	VSS
143	I/O	D[25] (D[1])
144	—	VDDLS
145	I/O	D[24] (D[0])
146	I/O	D[23] (D[15])
147	—	VDDH
148	I/O	D[22] (D[14])
149	—	VSS
150	I/O	D[21] (D[13])
151	—	VDDH
152	I/O	D[20] (D[12])
153	I/O	D[19] (D[11])
154	—	VSS
155	I/O	D[18] (D[10])
156	—	VDDLS

NO.	I/O	SIGNAL NAME
157	I/O	D[17] (D[9])
158	—	VSS
159	I/O	D[16] (D[8])
160	—	VDDH
161	I/O	IO[4]
162	O	CS0*
163	O	RD*
164	—	VSS
165	—	VDDLS
166	O	DGRNT*
167	I	DREQ*
168	O	ALE
169	O	WE*
170	—	VDDH
171	I/O	A[12]
172	I/O	A[11]
173	—	VSS
174	I/O	A[10]
175	I/O	A[9]
176	—	VDDL
177	I/O	A[8]
178	I/O	A[7]
179	—	VSS
180	I/O	A[6]
181	I/O	A[5]
182	—	VDDH
183	I/O	A[4]
184	—	VSS
185	I/O	A[3]
186	I/O	A[2]
187	—	VDDL
188	I/O	A[1]
189	I/O	A[0]
190	—	VSS
191	—	VSS
192	O	DCS0*
193	O	RAS1*
194	O	RAS0*
195	O	CAS3* (CAS0*)
196	—	VDDH
197	O	CAS2* (CAS1*)
198	O	CAS1* (CAS2*)
199	O	CAS0* (CAS3*)
200	—	VSS
201	—	VDDL
202	O	DCKE
203	—	VSS
204	I	DCLKIN
205	O	DCLKOUT
206	—	VDDH
207	O	DQMH
208	O	DQML

* Active-low signal

( ) indicates the signal name in the Little endian mode

4.2 PIN FUNCTIONS

- Memory Pins

NAME	I/O	DESCRIPTION
D[31:0]	I/O	These pins are the data bus for the system. 16-bit SDRAMs and DRAMS should be connected to bits 15:0. All other 16-bit ports should be connected to bits 31:16. Of course, 32-bit ports should be connected to be bits 31:0. These pins are normally outputs and only become inputs during reads, thus no resistors are required since the bus will only float for a short period of time during bus turn-around.
A[12:0]	O	These pins are the address bus for the system. The address lines are multiplexed and can be connected directly to SDRAM and DRAM devices. To generate the full 26-bit address for static devices, an external latch must be used to latch the signals using the ALE signal. For static devices, address bits 25:13 are provided by the external latch and address bits 12:0 (directly connected from the TMPR3922U's address bus) are held afterward by the TMPR3922U for the remainder of the address bus cycle.
ALE	O	This pin is used as the address latch enable to latch A[12:0] using an external latch, for generating the upper address bits 25:13.
RD*	O	This pin is used as the read signal for static devices. This signal is asserted for reads from MC3*-0*, CS3*-0*, CARD2CS*, and CARD1CS for memory and attribute space, and for reads from the TMPR3922U accesses if SHOWDINO is enabled (for debugging purposes).
WE*	O	This pin is used as the write signal for system. This signal is asserted for writes to MC3*-0*, CS3*-0*, CARD2CS* and CARD1CS for memory and attribute space, and for write to DRAM and SDRAM.
CAS0*(WE0*)	O	This pin is used as the CAS signal for SDRAMs, the CAS signal for D[7:0] for DRAMs, and the write enable signal for D[7:0] for static devices.
CAS1*(WE1*)	O	This pin is used as the CAS signal for D[15:8] for DRAMs, and the write enable signal for D[15:8] for static devices.
CAS2*(WE2*)	O	This pin is used as the CAS signal for D[23:16] for DRAMs, and the write enable signal for D[23:16] for static devices.
CAS3*(WE3*)	O	This pin is used as the CAS signal for D[31:24] for DRAMs, and the write enable signal for [31:24] for static devices.
RAS0*	O	This pin is used as the RAS signal for SDRAMs and the RAS signal for Bank0 SDRAMs.
RAS1*(DCS1*)	O	This pin is used as the chip select signal for Bank1 DRAMs and the RAS signal for Bank1 DRAMs.
DCS0*	O	This pin is used as the chip select signal for Bank0 SDRAMs.
DCKE	O	This pin is used as the clock enable for SDRAMs.
DCLKIN	I	This pin must be tied externally to the DCLKOUT signal and is used to match skew for the data input when reading from SDRAM and DRAM devices.
DCLKOUT	O	This pin is the (nominal) 82.944MHz clock for the SDRAMs.
DQMH	O	This pin is the upper data mask for a 16-bit SDRAM configuration.
DQML	O	This pin is the lower data mask for a 16-bit SDRAM or an 8-bit SDRAM configuration.
CS3-0*	O	These pins are the Chip Select 3 through 0 signals. They can be configured to support either 32-bit or 16-bit ports.
MCS1-0*	O	These pins are the chip select 1 through 0 signals for the external device. They can be configured to support either 32-bit or 16-bit ports.
CARD2CSH*, L*	O	These pins are the Chip Select signals for PCMCIA card slot 2.
CARD1CSH*, L*	O	These pins are the Chip Select signals for PCMCIA card slot 1.
CARDREG*	O	This pin is the REG* signal for the PCMCIA cards.
CARDIORD*	O	This pin is the IORD* signal for the PCMCIA IO cards.
CARDIOWR*	O	This pin is the IOWR* signal for the PCMCIA IO cards.
CARDDIR*	O	This pin is used to provide the direction control for bi-directional data buffers used for the PCMCIA slot(s). This signal will assert whenever CARD2CSH* or CARD2CSL* or CARD1CSH* or CARD1CSL* is asserted and a read transaction is taking place.
CARD2WAIT*	I	This pin is the card wait signal from PCMCIA card slot 2.
CARD1WAIT*	I	This pin is the card wait signal from PCMCIA card slot 1.
MCS1WAIT*	I	This pin is the wait signal from the external device 1.
MCS0WAIT*	I	This pin is the wait signal from the external device 0.

* Active-low signal

- Bus Arbitration Pins

NAME	I/O	DESCRIPTION
DREQ*	I	This pin is used to request external arbitration. If the TESTAIU signal is high and the TESTAIU function has been enabled, then once DGRNT* is asserted, external logic can initiate reads or writes to the TMPR3922U registers by driving the appropriate input signals. If the TESTAIU signal is low or the TESTAIU function has not been enabled, then the TMPR3922U memory transactions are halted and certain memory signals will be tri-stated when DGRNT* is asserted in order to allow an external master to access memory.
DGRNT*	O	This pin is asserted in response to DREQ* to inform the external test logic or bus master that it can now begin to drive signals.

* Active-low signal

- Clock Pins

NAME	I/O	DESCRIPTION
SYSCLKIN	I	This pin should be connected along with SYSCLKOUT to an external crystal which is the main TMPR3922U clock source.
SYSCLKOUT	O	This pin should be connected along with SYSCLKIN to an external crystal which is the main TMPR3922U clock source.
C32KIN	I	This pin alogn with C32KOUT should be connected to a 32.768kHz crystal.
C32KOUT	O	This pin along with C32KIN should be connected to a 32.768kHz crystal.
C6MIN	I	This pin along with C6MOUT should be connected to a 6MHz crystal.
C6MOUT	O	This pin along with C6MIN should be connected to a 6MHz crystal.
C48MOUT	O	This pin is a buffered output of the 48MHz clock.
BC32K	O	This pin is a buffered output of the 32.768kHz clock.
BCLK	O	This pin is a reference clock for the external device.

- CHI Pins

NAME	I/O	DESCRIPTION
CHIFS	I/O	This pin is the CHI frame synchronization signal. This pin is available for use in one of two modes. As an output, this pin allows the TMPR3922U to be the master CHI sync source. As an input, this pin allows an external peripheral to be the master CHI sync source and the TMPR3922U CHI module will slave to this external sync.
CHICLK	I/O	This pin is the CHI clock signal. This pin is available for use in one of two modes. As an output, this pin allows the TMPR3922U to be the master CHI clock source. As an input, this pin allows an external peripheral to be the master CHI clock source and the TMPR3922U CHI module will slave to this external clock.
CHIDOUT	O	This pin is the CHI serial data output signal.
CHIDIN	I	This pin is the CHI serial data inaut signal.

- IO Pins

NAME	I/O	DESCRIPTION
IO[6:0]	I/O	These pins are general purpose input/output ports. Each port can be independently programmed as an input or output port Each port can generate a separate positive and negative edge interrupt. Each port can also be independently programmed to use a 16 to 24ms debouncer.

- Reset Pins

NAME	I/O	DESCRIPTION
CPURES*	I	This pin is used to reset the CPU core. This pin should be connected to a switch for initiating a reset in the event that a software problem might hang the CPU core. The pin should also be pulled up to VSTANDBY† through an external pull-up resistor.
PON*	I	This pin serves as the Power On Reset signal for the TMPR3922U. This signal must remain low when VSTANDBY is asserted until VSTANDBY is stable. Once VSTANDBY† is asserted, this signal should never go low unless all power is lost in the system.

†VSTANDBY: This signal provides power for the TMPR3922U and other components in the system that must never lose power. This signal should always be asserted if there is either a good Main Backup Battery, or if a Battery Charger is plugged in.

- Power Supply Pins

NAME	I/O	DESCRIPTION
ONBUTN	I	This pin is used as the On Button for the system. Asserting this signal will cause PWRCS to set to indicate to the System Power Supply to turn power on to the system. PWRCS will not assert if the PWROK signal is low.
PWRCS	O	This pin is used as the chip select for the System Power Supply. When the system is off, the assertion of this signal will cause the System Power Supply to turn VCCDRAM†† and VCC3 on to power up the system. The Power Supply will latch SPI commands on the falling edge of PWRCS.
PWROK	I	This pin provides a status from the System Power Supply that there is a good source of power in the system. This signal typically will be asserted if there is a Battery Charger supplying current or if the Main Battery is good and the Battery Door is closed. If PWROK is low when the system is powered off, PWRCS will not assert as a result of the user pressing the ONBUTN or an interrupt attempting to wake up the system. If the device is on when the PWROK signal goes low, the software will immediately shut down the system since power is about to be lost. When PWROK goes low, there must be ample warning so that the software can shut down the system before power is actually lost.
PWRINT	I	This pin is used by the System Power Supply to alert the software that some status has changed in the System Power Supply and the software should read the status from the System Power Supply to find out what has changed. These will be low priority events, unlike the PWROK status, which is a high priority emergency case.
VCC3	I	This pin provides the status of the power supply for the ROM, TC35143F, system buffers, and other transient components in the system. This signal will be asserted by the System Power Supply when PWRCS is asserted, and will always be turned off when the system is powered down.

††VCCDRAM: This signal provides power for the DRAM and/or SDRAM. This supply must be off when VSTANDBY is first asserted, and remain off until the system is powered up by the assertion of PWRCS. When the software subsequently powers down the system it may choose keep this supply on to preserve the contents of memory.

- SIB Pins

NAME	I/O	DESCRIPTION
SIBDIN	I	This pin contains the input data shifted from TC35143F and/or external codec device.
SIBDOUT	O	This pin contains the output data shifted to TC35143F and/or external codec device.
SIBSCLK	O	This pin is the serial clock sent to TC35143F and/or external codec device. The programmable SIBSCLK rate is derived by dividing down from SIBMCLK.
SIBSYNC	O	This pin is the frame synchronization signal sent to TC35143F and/or external codec device. This frame sync is asserted for one clock cycle immediately before each frame starts and all devices connected to the SIB monitor SIBSYNC to determine when they should transmit or receive data.
SIBIRQ	I	This pin is a general purpose input port used for the SIB interrupt source from BETTY. This interrupt source can be configured to generate an interrupt on either a positive and/or negative edge.
SIBMCLK	I/O	This pin is the master clock source for the SIB logic. This pin is available for use in one of two modes. First, SIBMCLK can be configured as a high-rate output master clock source required by certain external codec devices. In this mode all SIB clock are synchronously slaved to the main TMPR3922U system clock CLK2X. Conversely, SIBMCLK can be configured as an input slave clock source. In this mode, all SIB clocks are derived from an external SIBMCLK oscillator source, which is asynchronous with respect CLK2X. Also, for this mode, SIBMCLK can still be optionally used as a high-rate master clock source required by certain external codec devices.

- SPI Pins

NAME	I/O	DESCRIPTION
SPICLK	I/O	This pin is used to clock data in and out of either the SPI master or slave device. This pin is the master clock source for the SPI logic. This pin is available for use in one of two modes. First, SPICLK can be configured as a master clock source required by certain external devices. In this mode all SPI clocks are synchronously slaved to the main TMPR3922U system clock FREECLK. Conversely, SPICLK can be configured as an input slave clock source. In this mode, all SPI clocks are derived from an external oscillator source, which is asynchronous with respect to FREECLK.
SPIOUT	O	This pin contains the data that is shifted into the SPI slave device.
SPIIN	I	This pin contains the data that is shifted out the SPI slave device.

- UART and SIR/FIR Pins

NAME	I/O	DESCRIPTION
TXD	O	This pin is the UART transmit signal from the UARTA module.
RXD	I	This pin is the UART receive signal to the UARTA module.
IROUT	O	This pin is the UART transmit signal from the UARTB module or the Consumer IR output signal if Consumer IR mode is enabled.
IRINA	I	This pin is the SIR receiver signal to the IRDA (FIR/SIR) module.
IRINB	I	This pin is the FIR receive signal to the IRDA (FIR/SIR) module.
RXPWR	O	This pin is the receiver power output control signal to the external communication IR analog circuitry.
CARDET	I	This pin is the UART receive signal to the UARTB module or is the carrier detect input signal from the external communication IR analog circuitry if consumer IR module is enabled.
FIROUT	O	This pin is the FIR/SIR transmit signal from the IRDA (FIR/SIR) module.

- Endianess Pins

NAME	I/O	DESCRIPTION
ENDIAN	I	This pin is used to select the endianess of the TMPR3922U. The "1" level input sets the endianess to the big endian, while the "0" level input to the little endian.

- Test Pins

NAME	I/O	DESCRIPTION
TESTAIU	I	This pin is used to define if the Boot ROM is 16 or 32 bits wide. If the TESTAIU pin is asserted during reset, the BIU will assume a 32-bit Boot ROM. The TESTAIU pin should remain static (either high or low).
TESTCPU	I	This pin is used for debugging purposes only. Then the TESTCPU should not be asserted.
TESTIN	I	This pin is used for debugging purposes only. Then the TESTIN should not be asserted.

- Spare Pins

NAME	I/O	DESCRIPTION
RESERVED	NC	These pins are reserved for future use and should be left unconnected.

- Power Supply Pins

NAME	I/O	DESCRIPTION
VDDH	V	These pins are the power pins for the TMPR3922U. (+3.3V)
VDDL	V	These pins are the power pins for the TMPR3922U. (+2.7V)
VDDLS	V	These pins are the power pins for the TMPR3922U. (+2.7V) In the suspend mode these pins should be 0V.
VSS	G	These pins are the ground pins for the TMPR3922U.
VDDP(for PLL)	V	This pin is the analog power pin for the TMPR3922U. Keep away from other VDD.
VSSP(for PLL)	G	This pin is the analog ground pin for the TMPR3922U. Keep away from other VSS.

4.3 PIN USAGE INFORMATION

This section contains tables summarizing various aspects of the usage for the TMPR3922U. TABLE 4.3a lists the standard versus multi-function usage for each TMPR3922U pin, if applicable. Those signal names shown in parentheses are test signals for debugging purposes only. The column showing the multi-function select signal and reset state indicates the internal control signal used to select the multi-function mode, as well as the default configuration of each multi-function pin during reset. The "Bus Arb State" column shows which pins are tri-stated whenever the DGRNT* signal is asserted in response to a DREQ* (external bus arbitration request).

TABLE 4.3a TMPR3922U STANDARD and MULTI-FUNCTION PIN USAGE

TMPR3912 pin	Standard Function (I=input, O=output)	Multi-function	Multi-function select (Reset State: 1=multi-function mode selected; 0=standard function & mode selected)	Bus Arb State
D[31:0]	D[31:0](I/O)			Hi-Z
A[12:0]	A[12:0](I/O)			
ALE	ALE(O)			Hi-Z
RD*	RD*(O)			Hi-Z
WE*	WE*(O)			Hi-Z
CAS0*(WE0*)	CAS0*(O)			Hi-Z
CAS1*(WE1*)	CAS1*(O)			Hi-Z
CAS2*(WE2*)	CAS2*(O)			Hi-Z
CAS3*(WE3*)	CAS3*(O)			Hi-Z
RAS0*	RAS0*(O)			Hi-Z
RAS1*(DCS1*)	RAS1*(O)			Hi-Z
DCS0*	DCS0(O)*			Hi-Z
DCKE	DCKE(O)			Hi-Z
DCLKIN	DCLKIN(I)			
DCLKOUT	DCLKOUT(O)			Hi-Z
DQMH	DQMH(O)			Hi-Z
DQML	DQML(O)			Hi-Z
DREQ*	DREQ*(I)	MIO[27]	MIOSEL[27](0)	
DGRNT*	DGRNT*(O)	MIO[26]	MIOSEL[26](0)	
SYSCLKIN	SYSCLKIN(I)			
SYSCLKOUT	SYSCLKOUT(O)			
C32KIN	C32KIN(I)			
C32KOUT	C32KOUT(O)			
C6MIN	C6MIN(I)			
C6MOUT	C6MOUT(O)			
C48MOUT	C48MOUT(O)			
BC32K	BC32K(O)	MIO[25]	MIOSEL[25](1)	
BCLK	BCLK(O)			
PWRCS	PWRCS(O)			
PWRINT	PWRINT(I)			
PWROK	PWROK(I)			
ONBUTN	ONBUTN(I)			
CPURES*	CPURES*(I)			
PON*	PON*(I)			
TXD	TXD(O)	MIO[24]	MIOSEL[24](0)	
RXD	RXD(I)	MIO[23]	MIOSEL[23](0)	
CS0*	CS0*(O)			Hi-Z
CS1*	CS1*(O)	MIO[22]	MIOSEL[22](0)	
CS2*	CS2*(O)	MIO[21]	MIOSEL[21](0)	
CS3*	CS3*(O)	MIO[20]	MIOSEL[20](0)	
MCS0*	MCS0*(O)	MIO[19]	MIOSEL[19](0)	
MCS1*	MCS1*(O)	MIO[18]	MIOSEL[18](0)	
MCS0WAIT*	MCS0WAIT*(I)	MIO[0]	MIOSEL[0](0)	
MCS1WAIT*	MCS1WAIT*(I)	MIO[1]	MIOSEL[1](0)	

TMPR3912 pin	Standard Function (I=input, O=output)	Multi-function	Multi-function select (Reset State: 1=multi-function mode selected; 0=standard function & mode selected)	Bus Arb State
CHIFS	CHIFS(I/O)	MIO[31]	MIOSEL[31](1)	
CHICLK	CHICLK(I/O)	MIO[30]	MIOSEL[30](1)	
CHIDOUT	CHIDOUT(O)	MIO[29]	MIOSEL[29](1)	
CHIDIN	CHIDIN(I)	MIO[28]	MIOSEL[28](1)	
VCC3	VCC3(I)			
IO15	IO15(I/O)			
IO14	IO14(I/O)			
IO13	IO13(I/O)			
IO12	IO12(I/O)			
IO11	IO11(I/O)			
IO10	IO10(I/O)			
IO9	IO9(I/O)			
IO8	IO8(I/O)			
IO7	IO7(I/O)			
IO6	IO6(I/O)			
IO5	IO5(I/O)			
IO4	IO4(I/O)			
IO3	IO3(I/O)			
IO2	IO2(I/O)			
IO1	IO1(I/O)			
IO0	IO0(I/O)			
SPICLK	SPICLK(O)	MIO[15]	MIOSEL[15](0)	
SPIOUT	SPIOUT(O)	MIO[14]	MIOSEL[14](0)	
SPIIN	SPIIN(I)	MIO[13]	MIOSEL[13](0)	
SIBSYNC	SIBSYNC(O)			
SIBDOUT	SIBDOUT(O)			
SIBDIN	SIBDIN(I)			
SIBMCLK	CIBMCLK(I/O)	MIO[12]	MIOSEL[12](0)	
SIBSCLK	SIBSCLK(O)			
SIBIRQ	SIBIRQ(I)			
RXPWR	RXPWR(O)	MIO[17]	MIOSEL[17](1)	
CARDET	CARDET(I)	MIO[16]	MIOSEL[16](1)	
IROUT	IROUT(O)			
IRINA	IRINA(I)			
IRINB	IRINB(I)			
FIROUT	FIROUT(O)			
TESTAIU	TESTAIU(I)			
TESTCPU	TESTCPU(I)			
TESTIN	TESTIN(I)			
CARDREG*	CARDREG*(O)	MIO[11]	MIOSEL[11](1)	
CARDIOWR*	CARDIOWR(O)	MIO[10]	MIOSEL[10](1)	
CARDIORD*	CARDIORD*(O)	MIO[9]	MIOSEL[9](1)	
CARD1CSL*	CARD1CSL*(O)	MIO[8]	MIOSEL[8](1)	
CARD1SCH*	CARD1CSH*(O)	MIO[7]	MIOSEL[7](1)	
CARD2CSL*	CARD2CSL*(O)	MIO[6]	MIOSEL[6](1)	
CARD2CSH*	CARD2CSH*(O)	MIO[5]	MIOSEL[5](1)	
CARD1WAIT*	CARD1WAIT*(I)	MIO[4]	MIOSEL[4](1)	
CARD2WAIT*	CARD2WAIT*(I)	MIO[3]	MIOSEL[3](1)	
CARDDIR*	CARDDIR*(O)	MIO[2]	MIOSEL[2](1)	
ENDIAN	ENDIAN(I)			
VDDH	+3.3V			
VDDL	+2.7V			
VDDLS	+2.7V/GND			
VDDP	+2.7V			
VSS	GND			
VSSP	GND			

TABLE 4.3b lists various power-down states and conditions for each TMPR3922U pin. The "Power-Down Control" column shows the conditions which trigger a power-down for each respective pin. This column also shows the reset state for each of these conditions.

The "PON* state" column defines the state of each pin at power-on reset (PON*). This condition is defined as initial power up of the TMPR3922U, whereby the TMPR3922U is initialized and the TMPR3922U pins are reset to the state shown in the table. This state is entered after power is applied for the very first time (VSTANDBY is turned on but VCC3 is still turned off).

The "1st-time power-up state" column defines the state of each pin after power-up mode (RUNNING STATE) is executed for the first times. This mode is defined as VCC3 applied to the entire system and is initiated by the user pressing the ONBUTN while in the power-on reset (PON*) state. Note that the defined state of various pins for 1st-time power-up may depend on the configuration of external devices attached to these pins. After 1st-time power-up, the software could change the state of various pins to be different from those shown in the table. Thereafter, subsequent transitions from SLEEP STATE to RUNNING STATE might result in different states for these pins.

The "Power-down state" column defines the state of each pin during power-down mode (SLEEP STATE). This mode is defined as VCC3 turned off to the entire system, except for the TMPR3922U (RTC and interrupts alive) and any persistent memory.

TABLE 4.3b TMPR3922 POWER-DOWN PIN USAGE

TMPR3922 pin	Power-Down Control powerdown=(vccon & vcc3)* (reset state)	PON* state	1st time power-up state	power-down state
D[31:0]	MEMPOWERDOWN	LOW	LOW	LOW
A[12:0]	MEMPOWERDOWN	LOW	LOW	LOW
ALE		LOW	LOW	LOW
RD*	POWERDOWN	LOW	HI	LOW
WE*	MEMPOWERDOWN	LOW	LOW	LOW
CAS0*(WE0*)	MEMPOWERDOWN	LOW	LOW	LOW
CAS1*(WE1*)	MEMPOWERDOWN	LOW	LOW	LOW
CAS2*(WE2*)	MEMPOWERDOWN	LOW	LOW	LOW
CAS3*(WE3*)	MEMPOWERDOWN	LOW	LOW	LOW
RAS0*	MEMPOWERDOWN	LOW	LOW	LOW
RAS1*(DCS1*)	MEMPOWERDOWN	LOW	LOW	LOW
DCS0*	MEMPOWERDOWN	LOW	LOW	LOW
DCKE	MEMPOWERDOWN	LOW	LOW	LOW
DCLKIN				
DCLK0UT	MEMPOWERDOWN	LOW	LOW	LOW
DQMH	MEMPOWERDOWN	LOW	LOW	LOW
DQML	MEMPOWERDOWN	LOW	LOW	LOW
DREQ*	POWERDOWN & MIOPD[27](1)	PULL-DOWN	IN	SELECTABLE
DGRNT*	POWERDOWN & MIOPS[26](0)	LOW	HI	SELECTABLE
SYSCLKIN	POWERDOWN	OSC OFF	OSC ON	OSC OFF
SYSCLKOUT	POWERDOWN	OSC OFF	OSC ON	OSC OFF
C32KIN		OSC ON	OSC ON	OSC ON
C32K0UT		OSC ON	OSC ON	OSC ON
C6MIN	POWERDOWN	OSC OFF	OSC ON	OSC OFF
C6MOUT	POWERDOWN	OSC OFF	OSC ON	OSC OFF
C48M0UT	POWERDOWN	LOW	LOW	LOW
BC32K	POWERDOWN & MIOPD[25](1)	PULL-DOWN	IN	SELECTABLE
BCLK	POWERDOWN	LOW	LOW	LOW
PWRCS		LOW	HI	LOW
PWRINT				
PWROK				
ONBUTN				
CPURES*				
PON*				
TXD	POWERDOWN & MIOPD[24](O)	LOW	LOW	SELECTABLE
RXD	POWERDOWN & MIOPD[23](1)	PULL-DOWN	IN	SELECTABLE
CS0*	POWERDOWN	PULL-DOWN	HI	PULL-DOWN
CS1*	POWERDOWN & MIOPD[22](1)	PULL-DOWN	HI	SELECTABLE
CS2*	POWERDOWN & MIOPD[21](1)	PULL-DOWN	HI	SELECTABLE
CS3*	POWERDOWN & MIOPD[20](1)	PULL-DOWN	HI	SELECTABLE
MCS0*	POWERDOWN & MIOPD[19] (0)	IN	IN	SELECTABLE
MCS1*	POWERDOWN & MIOPD[18](0)	IN	IN	SELECTABLE
MCS0WAIT*	POWERDOWN & MIOPD[1](0)	IN	IN	SELECTABLE

TMPR3922 pin	Power-Down Control powerdown=(vccon & vcc3)* (reset state)	PON* state	1st time power-up state	power-down state
MCS1WAIT*	POWERDOWN & MIOPD[0](0)	IN	IN	SELECTABLE
CHIFS	POWERDOWN & MIOPD[31](1)	PULL-DOWN	IN	SELECTABLE
CHICLK	POWERDOWN & MIOPD[30](1)	PULL-DOWN	IN	SELECTABLE
CHIDOUT	POWERDOWN & MIOPD[29](1)	PULL-DOWN	IN	SELECTABLE
CHIDIN	POWERDOWN & MIOPD[28](1)	PULL-DOWN	IN	SELECTABLE
VCC3	POWERDOWN	PULL-DOWN		PULL-DOWN
IO15	POWERDOWN & IOPD[15](1)	PULL-DOWN	IN	SELECTABLE
IO14	POWERDOWN & IOPD[14](1)	PULL-DOWN	IN	SELECTABLE
IO13	POWERDOWN & IOPD[13](1)	PULL-DOWN	IN	SELECTABLE
IO12	POWERDOWN & IOPD[12](1)	PULL-DOWN	IN	SELECTABLE
IO11	POWERDOWN & IOPD[11](1)	PULL-DOWN	IN	SELECTABLE
IO10	POWERDOWN & IOPD[10](1)	PULL-DOWN	IN	SELECTABLE
IO9	POWERDOWN & IOPD[9](1)	PULL-DOWN	IN	SELECTABLE
IO8	POWERDOWN & IOPD[8](1)	PULL-DOWN	IN	SELECTABLE
IO7	POWERDOWN & IOPD[7](1)	PULL-DOWN	IN	SELECTABLE
IO6	POWERDOWN & IOPD[6](1)	PULL-DOWN	IN	SELECTABLE
IO5	POWERDOWN & IOPD[5](1)	PULL-DOWN	IN	SELECTABLE
IO4	POWERDOWN & IOPD[4](1)	PULL-DOWN	IN	SELECTABLE
IO3	POWERDOWN & IOPD[3](1)	PULL-DOWN	IN	SELECTABLE
IO2	POWERDOWN & IOPD[2](1)	PULL-DOWN	IN	SELECTABLE
IO1	POWERDOWN & IOPD[1](1)	PULL-DOWN	IN	SELECTABLE
IO0	POWERDOWN & IOPD[0](1)	PULL-DOWN	IN	SELECTABLE
SPICLK	POWERDOWN & MIOPD[15](0)	LOW	LOW	SELECTABLE
SPIOUT	POWERDOWN & MIOPD[14](0)	LOW	LOW	SELECTABLE
SPIIN	POWERDOWN & MIOPD[13](1)	PULL-DOWN		SELECTABLE
SIBSYNC	POWERDOWN	LOW	LOW	LOW
SIBDOUT	POWERDOWN	LOW	LOW	LOW
SIBDIN	POWERDOWN	PULL-DOWN		PULL-DOWN
SIBMCLK	POWERDOWN & MIOPD[12](1)	PULL-DOWN	IN	SELECTABLE
SIBSCLK	POWERDOWN	LOW	LOW	LOW
SIBIRQ	POWERDOWN	PULL-DOWN		PULL-DOWN
RXPWR	POWERDOWN & MIOPD[17](0)	PULL-DOWN	IN	SELECTABLE
CARDET	POWERDOWN	PULL-DOWN	X	SELECTABLE
IROUT	POWERDOWN & MIOPD[16](0)	PULL-DOWN	IN	SELECTABLE
IRINA	POWERDOWN	PULL-DOWN	X	PULL-DOWN
IRINB	POWERDOWN	PULL-DOWN	X	PULL-DOWN
FIROUT	POWERDOWN	LOW	LOW	LOW
TESTAIU				
TESTCPU				
TESTIN				
CARDREG*	POWERDOWN & MIOPD[11](1)	PULL-DOWN	IN	SELECTABLE
CARDIOWR*	POWERDOWN & MIOPD[10](1)	PULL-DOWN	IN	SELECTABLE
CARDIORD*	POWERDOWN & MIOPD[9](1)	PULL-DOWN	IN	SELECTABLE
CARD1CSL*	POWERDOWN & MIOPD[8](1)	PULL-DOWN	IN	SELECTABLE
CARD1CSH*	POWERDOWN & MIOPD[7](1)	PULL-DOWN	IN	SELECTABLE
CARD2CSL*	POWERDOWN & MIOPD[6](1)	PULL-DOWN	IN	SELECTABLE
CARD2CSH*	POWERDOWN & MIOPD[5](1)	PULL-DOWN	IN	SELECTABLE
CARD1WAIT*	POWERDOWN & MIOPD[4](1)	PULL-DOWN	IN	SELECTABLE
CARD2WAIT*	POWERDOWN & MIOPD[3](1)	PULL-DOWN	IN	SELECTABLE
CARDDIR*	POWERDOWN & MIOPD[2](1)	PULL-DOWN	IN	SELECTABLE
ENDIAN				
VDDH				
VDDL				
VDDLS				
VDDP				
VSS				
VSSP				

5) FUNCTION SPECIFICATIONS

5.1 OUTLINE

The TMPR3922U consists of PDA system support logic, integrated with the TX3920 Processor Core designed by Toshiba.

5.2 TX3920 PROCESSOR CORE

The TX3920 processor core is a Toshiba-developed microprocessor core based on the R3000A RISC architecture developed by MIPS Group, a division of silicon Graphics, Inc. of the United States.

5.2.1 INSTRUCTIONS

All TX3920 Processor Core instructions are 32-bit instructions. Apart from some coprocessor instructions, the instructions are upwardly compatible with the R3000A. The TX3920 Processor Core instructions can be classified into six types.

- **Load and store instructions**

  Transfer data between memory and general-purpose registers.

- **Computational instructions**

  These include arithmetic, logical, shift, multiply, divide, and multiply-add instructions. The multiply-add instructions are extensions to the R3000A. The multiply instructions can also be used as three-operand instructions.

- **Special instructions**

  Used for system call or break point.

- **Jump and branch instructions**

  Change the control flow of a program. The Branch-Likely instruction is provided as an extension to the R3000A.

- **Coprocessor instructions**

  Perform operations for coprocessors. The R3000A LWCz and SWCz instructions are reserved instructions in the TX3920 Processor Core. Attempting execution generates a reserved instruction exception. Note that the COPz, CTCz and MTCz instructions are no-operation instructions, the CFCz and MFCz instructions load undefined data to general purpose registers (rt) in the TMPR3922U.

- **System control coprocessor instructions**

  Perform operations on the CP0 registers to manipulate the memory management and exception handing functions of the processor.

5.2.2 REGISTERS

- **The TX3920 Processor Core has following registers.**

  32 general purpose registers (32-bit)

- **HI/LO registers**

  Hold the result of multiply and divide operation

- **PC (Program Counter)**

- **Cause register**

  Indicates the nature of the most recent exception

- **EPC (Exception Program Counter) register**

  Holds the program counter at the time the exception occurred, indicating the address where processing is to resume after the exception processing is completed.

- **Status register**

  Holds the operating mode status (user mode or kernel mode), interrupt masking status, diagnosis status and other such information.

- **BadVAddr (Bad Virtual Address) register**

  Holds the most recent virtual address for which a virtual address translation error occurred.

- **PRId register**

  Shows the revision number of the TX3920 Processor Core.

- **Cache register**

  Controls the instruction cache (reserved) and the data cache autolock bits.

- **Config register**

  Some configuration options.

- **Context register**
- **Entry HI/LO register**
- **Index register**
- **Tag LO register**
- **Random register**

  TLB Random index.

- **Page mask register**

  Hold a comparison mask that sets the variable page size for each TLB entry.

- **Wired register**

  TLB wired boundary

- **Debug register**

  Control software debug exception.

- **DEPC**

  Program counter for software debug exception.

5.2.3 MEMORY MANAGEMENT

The TX3920 Processor Core has a 4G-byte memory address space. The 4G-byte memory space consists of a 2G-byte user area and a 2G-byte kernel area. The kernel area contains a cache area and an uncache area. The TX3920 Processor Core provides a full-featured memory management unit (MMU) utilizing an on-chip Translation Lookaside Buffer (TLB). The on-chip TLB majur characteristics are:

- 64 x 64-bit wide entries
- 4K/16K/64K/256K/1M/4M page size
- fully associative
- 2 entry micro TLB for instruction address translation
- instruction address translation accesses full TLB after micro-TLB miss
- data address translation accesses full TLB

5.2.4 PIPELINE

The TX3920 Processor Core pipeline consists of five stages. The pipeline configuration enables the TX3920 Processor Core to execute nearly all instructions in one clock.

5.2.5 CACHE

The TMPR3922U incorporates a 16K-byte instruction cache and a 8K-byte data cache. The instruction cache uses two-way set-associative mapping with a block size of 16 bytes. The data cache uses two-way set-associative mapping with a block size of four bytes. Both data and Instruction cache have a lock function that locks data in one direction. Either copy-back or write-through method is used to write data back to memory.

5.2.6 DSP FUNCTION

The TX3920 Processor Core has a high-speed multiplier/accumulator and supports 32-bit x 32-bit multiplier operations, with 64-bit accumulator in one cycle.

5.3 PERIPHERAL FUNCTIONS

5.3.1 CLOCK GENERATOR

The TMPR3922U uses an internal PLL and an external cystal oscillator to generate a clock with 16 times the input clock frequency. The PLL oscillation can be halted externally to reduce power dissipation.

5.3.2 WRITE BUFFER

The TMPR3922U incorporates a four-stage write buffer.

5.3.3 BUS INTERFACE UNIT (BIU) MODULE

The TMPR3922U has a Bus Interface Unit with the following features.

- **supports 2 Banks of SDRAM and/or DRAM (EDO)**
  - 16-bit or 32-bit SDRAM configuration
  - 16-bit or 32-bit DRAM (EDO) configuration
  - 4 Mbit, 16 Mbit and 64 Mbit parts supported
  - page mode reads and writes supported
  - independent refresh counters for each bank
  - self refreshing parts supported to retain memory when system is powered down

■ **4 general purpose chip selects (CS3*-CS0*)**
- 16-bit or 32-bit ports
- programmable wait states
- read page mode

■ **2 general purpose chip selects (MCS3*-MCS0*)**
- 16-bit or 32-bit ports
- programmable wait states
- read page mode
- WAIT signal supported

■ **2 full PCMCLA slots**
- 8-bit or 16-bit ports
- IORD and IOWR provided to support I/O cards
- WAIT signal supported

5.3.4 SYSTEM INTERFACE UNIT (SIU) MODULE

The TMPR3922U has a System Interface Unit with the following features.

- multi-channel 32-bit DMA controller
- independent DMA controller for SIB to/from TC35143F audio/telecom codecs, high-speed serial, port, IRDA, UART, and general purpose UART
- address decoding for the internal registers

5.3.5 CLOCK MODULE

The TMPR3922U has a Clock module with the following features.

- The TMPR3922U supports system-wide single crystal configuration, besides the 32 KHz RTC XTAL (reduces cost, power, and board space)
- common crystal rate divided to generate clock for CPU, sound, telecom, UARTs, etc.
- independent enabling of disabling of individual clocks under software control, for power management

5.3.6 CONCENTRATION HIGHWAY INTERFACE (CHI) MODULE

The TMPR3922U has a CHI module with the following features.

- high-speed serial Concentration Highway Interface (CHI) contains logic for interfacing to external full-duplex serial time-division-multiplexed (TDM) communication peripherals
- supports ISDN line interface chips and other PCM/TDM serial devices
- CHI interface is programmable (number of channels, frame rate, bit rate, etc.) to provide support for a variety of formats
- supports data rates up to 4.096 Mbps
- independent DMA support for CHI receive and transmit

5.3.7 INTERRUPT MODULE

The TMPR3922U has an Interrupt module with the following features.

- contains logic for individually enabling, reading, and clearing all TMPR3922U interrupt sources
- interrupts generated from internal TMPR3922U modules or from edge transitions on external signal pins

5.3.8 IO MODULE

The TMPR3922U has an IO module with the following features.

- contains support for reading and writing the 16 bi-directional general purpose IO pins and the 32 bi-directional multi-function IO pins
- each IO port can generate a separate positive and negative edge interrupt
- independently configurable IO ports allow the TMPR3922U to support a flexible and wide range of system applications and configurations

5.3.9 IR MODULE

The TMPR3922U has an IR module with the following features.

- IR consumer mode
  - allows control of consumer electronic devices such as stereos, TVs, VCRs, etc.
  - programmable pulse parameters
  - external analog LED circuitry
- IRDA communication mode
  - IrDA 1.0 mode with filter is supported (BOF and EOF are detected by hardware and the bit pattern which data translation is necessary is detected and translated by hardware.)
  - Also IrDA 1.1 compliance (2.4/9.6/19.2/38.4/57.6/115.2 kbps are available)
  - 1.152 Mbps NRZ supported
  - 4 Mbps 4ppm/single plus supported (512 kbps and 4 Mbps with double pluse are not supported)
  - CRC generation/check supported
  - Address filter mode supported
  - Power down mode (Power down register controls FIR clock to reduce power)
  - supported by the UART module within the TMPR3922U
  - external analog receiver preamp and LED circuitry
  - data rate = up to 115 kbps at 1 meter
- IR FSK communication mode
  - supported by the UART module within the TMPR3922U
  - external analog IR chip(s) perform frequency modulation to generate the desired IR communication mode protocol
  - data rate = up to 36000 bps at 3 meters
- carrier detect state machine
  - periodically enables IR receiver to check if a valid carrier is present

5.3.10 POWER MODULE

The TMPR3922U has a Power module with the following features.

- power-down modes for individual internal peripheral modules
- serial (SPI port) power supply control interface supported
- power management state machine has 3 states: RUNNING, DOZING and SLEEP

5.3.11 SERIAL INTERCONNECT BUS (SIB) MODULE

The TMPR3922U has a SIB module with the following features.

- The TMPR3922U contains holding and shift registers to support the serial interface to the TC35143F codec devices
- interface compatible with slave mode 3 of the Crystal CS4216 codec
- synchronous, frame-based protocol
- The TMPR3922U always master source of clock and frame frequency and phase; programmable clock frequency
- each SIB frame consists of 128 clock cycles, further divided into 2 subframes of words of 64 bits each (supports up to 2 device simultaneously)
- independent DMA support for audio receive and transmit, telecom receive and transmit
- supports 8-bit or 16-bit mono telecom formats
- supports 8-bit or 16-bit mono or stereo audio formats
- independently programmable audio and telecom sample rates
- CPU read/write registers for subframe control and status

5.3.12 SERIAL PERIPHERAL INTERFACE (SPI) MODULE

The TMPR3922U has an SPI module with the following features.

- provides interface to SPI peripherals and devices
- full-duplex, synchronous serial data transfers (data in, data out, and clock signals)
- The TMPR3922U supplies dedicated chip select and interrupt for an SPI interface serial power supply
- 8-bit or 16-bit data word lengths for the SPI interface
- programmable SPI baud rate

5.3.13 TIMER MODULE

The TMPR3922U has a Timer module with the following features.

- Real Time Clock (RTC) and Timer
- 43-bit counter (30.517 µs granularity); maximum uninterrupted time = 3104 days

- 43-bit alarm register (30.517 µs granularity)
- 16-bit periodic timer (0.868 µs granularity); maximum timeout = 56.8 ms
- interrupts on alarm, timer, and prior to RTC roll-over

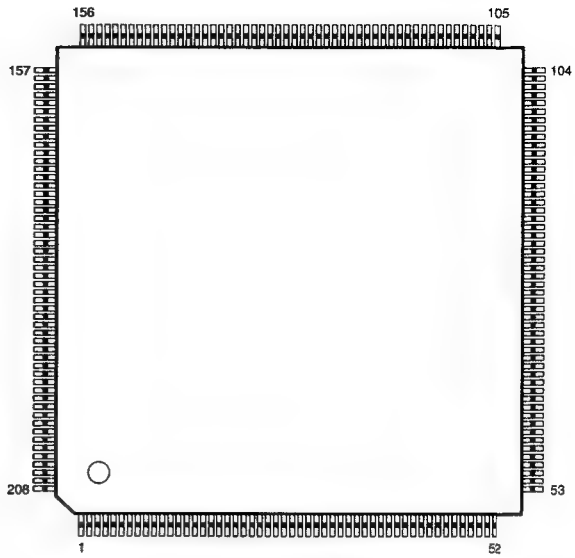
5.3.14 UART MODULE

The TMPR3922U has a UART module with the following features.

- 2 independent full-duplex UARTs
- programmable baud rate generator
- UARTA port used for general purpose serial control interface
- UARTB port used for serial control interface to external IR module
- UARTA and UARTB DMA support for receive and transmit

6) PACKAGE DIMENSION

6.1 TMPR3922U



PV-5000 CPU SETTING (USING THE PIN FOR PV-5000)

PIN		States after PON RESET	SHARP	SHARP I/O	PD Setting	DB Setting	External process
RAS0		LOW	RAS0	O			
RAS1		LOW	RAS1	O			
CAS0		LOW	CAS0	O			
CAS1		LOW	CAS1	O			
CAS2		LOW	CAS2	O			
CAS3		LOW	CAS3	O			
JTDI		—	NOT USE	—			
JTDO		—	NOT USE	—			
JTMS		—	NOT USE	—			
JTCK		—	NOT USE	—			
SYSCLKIN		OSC OFF	OSC	I			
SYSCLKOUT		OSC OFF	OSC	O			
C32KIN		OSC ON	OSC	I			
C32KOUT		OSC ON	OSC	O			
C6MIN		OSC OFF	OSC	I			
C6MOUT		OSC OFF	OSC	O			
C48MOUT		LOW	C48MOUT	O			
BCLK		LOW	BCLK	O			
PWRCS		LOW	PWRCS	O			
PWRINT		—	NOT USE	—			Pull Down
PWROK		—	POWER CONDITION OK SIGNAL	I			
ONBUTN		—	ON KEY INPUT	I			
CPURES		—	CPU CORE RESET INPUT	I			
PON		—	POWER ON RESET INPUT	I			
VCC3		Pull Down	VCC3	I	Pull Down		
IO15			RS232C EN	O	N	N	
IO14			MAIN BATTERY I/F CLK	O	N	N	
IO13			MAIN BATTERY I/F OUT	O	N	N	
IO12			MAIN BATTERY I/F IN	I	N	N	
IO11		Pull Down	NC (AC IN)	I	N	N	PU to VSTANDBY
IO10		Pull Down	DAA RING	I	N	N	PU to VSTANDBY
IO9		Pull Down	RESET for ANALOG chip & SED1354 & KBC	O	Y	N	
IO8		Pull Down	PPSH INTERRUPT	I	Y	N	PU to VCC3.3

PIN		States after PON RESET	SHARP	SHARP I/O	PD Setting	DB Setting	External process
IO7		Pull Down	SPK ON	O	Y	N	
IO6		Pull Down	UART-A CTS	I	N	N	
IO5		Pull Down	UART-A RTS	O	N	N	
IO4		Pull Down	MODEM EN or /DISEN	I	N	N	
IO3		Pull Down	NOT USE (NOTIFICATION LED STOP BUTTON)	I	N	Y	Pull Down
IO2		Pull Down	NOT USE (MAIN BATTERY DOOR OPEN)	I	N	Y	Pull Down
IO1		Pull Down	PC CARD 1 BVD	I	N	Y	
IO0		Pull Down	RESERVED (MIC REC BUTTON)	I	N	Y	Pull Down
MIO31	CHIFS	Pull Down	UART-A DTR (18PIN)	O	N	—	
MIO30	CHICLK	Pull Down	TABLET CHECK	O	Y	—	
MIO29	CHIDOUT	Pull Down	UART-A DCD (18PIN)	I	N	—	
MIO28	CHIDIN	Pull Down	ALARM lh IN	I	N	—	
MIO27	DREQ	Pull Down	LED GREEN ON	O	N	—	
MIO26	DGRNT	Pull Down	DRAM VCC ON	O	N	—	
MIO25	BC32K	Pull Down	BC32K (Clock for G.A)	O	N	—	
MIO24	TXD	LOW	UART-A TXD (18PIN)	O	N	—	
MIO23	RXD	Pull Down	UART-A RXD (18PIN)	I	N	—	
MIO22	CS1	Pull Down	TC6345 CS	O	Y	—	PU to VCC3.3
MIO21	CS2	Pull Down	4Mb FLASH CS	O	Y	—	PU to VCC3.3
MIO20	CS3	Pull Down	G.A CS	O	N	—	
MIO19	MCS0	Pull Down	SED1354 CS	O	Y	—	PU to VCC3.3
MIO18	MCS1	Pull Down	PPSH CS + Copy CS	O	Y	—	PU to VCC3.3
MIO17	RXPWR	Pull Down	IR ON	O	N	—	
MIO16	IROUT	Pull Down	OUTPUT IR FE	O	Y	—	
MIO15	SPICLK	LOW	NOT USE (RESERVE for POINTING)	O	N	—	
MIO14	SPIOUT	LOW	NOT USE (RESERVE for POINTING)	O	N	—	
MIO13	SPIIN	Pull Down	NOT USE (RESERVE for POINTING)	I	N	—	Pull Down
MIO12	SIBMCLK	Pull Down	KEY INTERRUPT (from G.A)	I	N	—	Pull Down
MIO11	CARDREG	Pull Down	CARDREG	O	Y	—	
MIO10	CARDIOWR	Pull Down	CARDIOWR	O	Y	—	
MIO09	CARDIORD	Pull Down	CARDIORD	O	Y	—	
MIO08	CARD1CSL	Pull Down	CARD1CSL	O	Y	—	
MIO07	CARD1CSH	Pull Down	CARD1CSH	O	Y	—	
MIO06	CARD2CSL	Pull Down	BL VCC ON	O	Y	—	
MIO05	CARD2CSH	Pull Down	LED RED ON	O	N	—	
MIO04	CARD1WAIT	Pull Down	CARD1WAIT	I	Y	—	PU to VCC3.3
MIO03	CARD2WAIT	Pull Down	B/U BATTERY CHECK	O	Y	—	
MIO02	CARDDIR	Pull Down	CARD INTERRUPT	I	N	—	Pull Down
MIO01	MCS1WAIT	Pull Down	PPSH WAIT	I	Y	—	PU to VCC3.3
MIO00	MCS0WAIT	Pull Down	SED1354 WAIT	I	Y	—	PU to VCC3.3
SIBSYNC		LOW	SIB	O	LOW		
SIBDOUT		LOW	SIB	O	LOW		
SIBDIN		Pull Down	SIB	I	Pull Down		
SIBSCLK		LOW	SIB	O	LOW		
SIBIRQ		Pull Down	SIB	I	Pull Down		
IRINA		Pull Down	NOT USE	I			Pull Down
IRINB		Pull Down	NOT USE	I			Pull Down
FIROUT		LOW	NOT USE	O	LOW		
CARDET		Pull Down	INPUT IR FE	I	Y		Pull Down
ENDIAN		LOW (conn to GND)	LOW (conn to GND)	I	—		
CS0		Pull Down	MASK ROM CS	O	Pull Down		

2-2. Analog Front end LSI (TC35143AF)

1. Outline

TC35143AF is an analog front end LSI suitable for personal digital assistants (PDA) including HPC. It consists of a V.34 modem telephone line interface, sound interface compatible with the handsfree/handset system, and touch screen interface. The communication with the host processor is performed through the SIB (Serial Interface Bus). The LSI is connectable to a master processor with an SIB interface. Clocks used inside the TC35143AF are generated from the serial transfer clocks of the SIB interface. There is no need for any clock oscillator. Sampling data, control signals and status of each interface block is communicated with the host processor through the SIB interface.

2. Features

2.1 Telephone line interface

- 16-bit ADC/DAC
- Programmable input amplifier gain (2-stage, in steps of 6dB)
- Full differential telephone line interface
- Analog echo canceller is incorporated
- Programmable sampling frequency (3-stage: 7.2 kHz, 8 kHz, 9.6 kHz)

2.2 Sound interface

- 14-bit ADC/DAC
- 2 mike input lines, 2 speaker output lines (supports handsfree, handset system)
- Power On/Off function for each block
- Mike input mute switch, speaker input mute switch
- Programmable mike amplifier gain (2 types: 15 stages in steps of 1.5 dB and 4 stages in steps of 6 dB)
- Programmable speaker output level attenuator (8 stages in steps of 3 dB)
- Programmable sampling frequency (4 stages in steps of 8 kHz, about 11.03 kHz, 16 kHz, about 22.05 kHz)

2.3 Touch screen interface

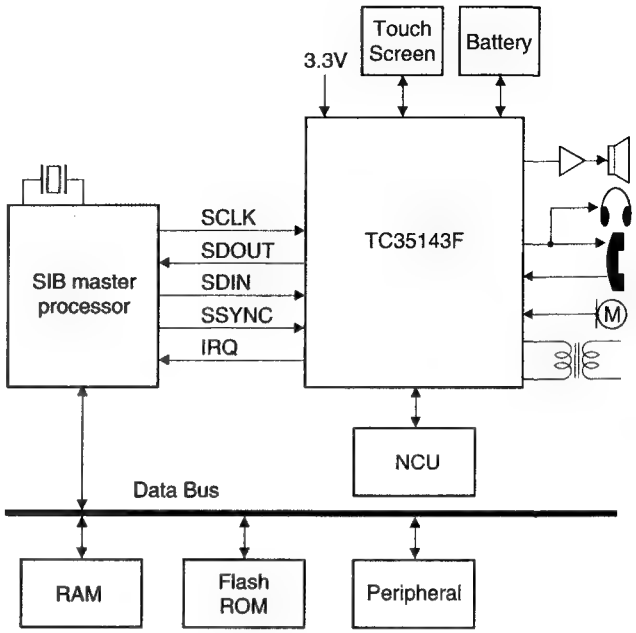
- Voltage measurement 10-bit ADC
- Touch starting mode from stand-by state
- Plate applied voltage generation circuit
- General-purpose analog input port (4 inputs)

2.4 Others

- Interrupt output port (programmable interrupt factor setting function)
- Multichip connection through SIB interface (SIB clock input fixed to 9.216 MHz)
- General-purpose I/O port (10 ch)
- +3.3 V battery power supply
- 64-pin QFP package

3. System block diagram

A typical system configuration is shown below.



4. Pin description

4.1 Pin configuration diagram

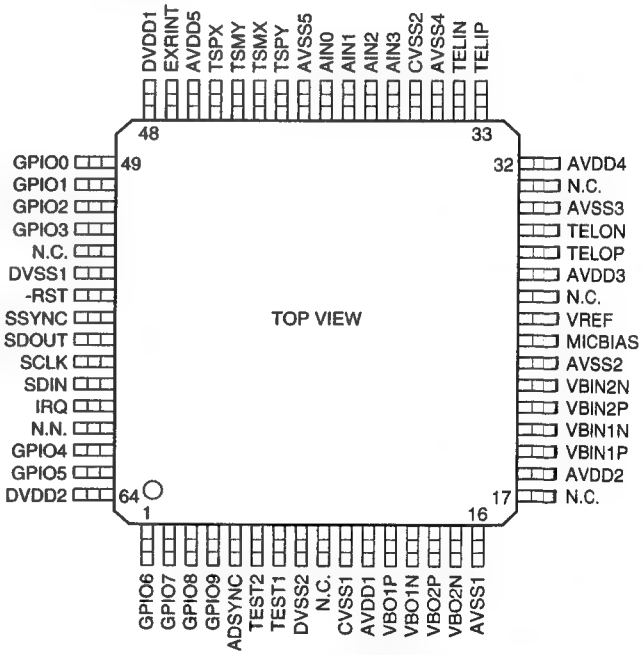


Fig. 4.1.A Pin diagram of TC35143AF

4.2 Pin function

Table 4.2.A TC35143AF pin functions

Symbol	Pin No.	A/D/P	I/O	DEF	Group	Description
SCLK	58	D	I	—	HOST	Serial data transfer clock. Serial data is transferred synchronizing with this clock. SCLK is used as the master clock for TC35143AF. The specification of SCLK is 9.216 MHz, with duty ratio 50%. Connect to the clock output of SIB master chip.
SSYNC	56	D	I	—	HOST	This signal provides synchronization for serial data frames. 72 kHz clock. 1 frame consists of 128 bits of serial data. Connect to the synchronizing signal output of SIB master chip.
SDIN	59	D	I	—	HOST	Serial input data terminal. Serial data input through the SDIN terminal is latched inside at the falling edge of SCLK. Connect to the data output of SIB master chip.
SDOUT	57	D	O	HZ	HOST	Serial output data terminal. Serial data output through SDOUT terminal is output, synchronizing with the rising edge of SCLK. Connect to the data input of SIB master chip.
IRQ	60	D	O	L	HOST	Interrupt output terminal. Interrupt factors output from the control resistor to this terminal are set. The signal level at the time of interrupt is active high.
–RST	55	D	I	—	HOST	System reset. This signal is active low.
TSPX	45	A	I/O	HZ (IN)	TSC	Interface terminal for touch screen X plate. Open when not in use.
TSMX	43	A	I/O	HZ (IN)	TSC	Interface terminal for touch screen X place. Open when not in use.
TSPY	42	A	I/O	HZ (IN)	TSC	Interface terminal for touch screen Y plate. Open when not in use.
TSMY	44	A	I/O	HZ (IN)	TSC	Interface terminal for touch screen Y plate. Open when not in use.
AIN0	40	A	I	—	ADC	General-purpose input terminal for 10-bit ADC. Open when not in use.
AIN1	39	A	I	—	ADC	General-purpose input terminal for 10-bit ADC. Open when not in use.
AIN2	38	A	I	—	ADC	General-purpose input terminal for 10-bit ADC. Open when not in use.
AIN3	37	A	I	—	ADC	General-purpose input terminal for 10-bit ADC. Open when not in use.
ADSYNC	5	D	I	—	ADC	Synchronizing clock input terminal when putting 10-bit ADC in the external clock synchronizing mode. ADC starts conversion synchronizing with the edge of ADSYNC. Pull down when not in use.
EXRINT	47	A	I	—	TSC	Terminal to which external resistance is connected, for adjusting detection sensitivity in touch detection mode. Connect a resistance of more than 16 kΩ between AVDD5.
TELOP	28	A	O	HZ	TEL	Positive polarity output terminal for telephone line CODEC
TELON	29	A	O	HZ	TEL	Negative polarity output terminal for telephone line CODEC
TELIP	33	A	I	—	TEL	Positive polarity input terminal for telephone line CODEC. Open when not in use.
TELIN	34	A	I	—	TEL	Negative polarity input terminal for telephone line CODEC. Open when not in use.
VBO1P	12	A	O	HZ	VB	Positive polarity output terminal 1 for sound CODEC. It is used for the handset speaker.
VBO1N	13	A	O	HZ	VB	Negative polarity output terminal 1 for sound CODEC. It is used for the handset speaker.
VBO2P	14	A	O	HZ	VB	Positive polarity output terminal 2 for sound CODEC. It is used for the external speaker.
VBO2N	15	A	O	HZ	VB	Negative polarity output terminal 2 for sound CODEC. It is used for the external speaker.
VB1N1P	19	A	I	—	VB	Positive polarity input terminal 1 for sound CODEC. It is used for the hand mike. Open when not in use.
VBIN1N	20	A	I	—	VB	Negative polarity input terminal 1 for sound CODEC. It is used for the hand mike. Open when not in use.
VBIN2P	21	A	I	—	VB	Positive polarity input terminal 2 for sound CODEC. It is used for the external mike. Open when not in use.
VBIN2N	22	A	I	—	VB	Negative polarity input terminal 2 for sound CODEC. It is used for the external mike. Open when not in use.
MICBIAS	24	A	O	HZ	VB	This is a power supply terminal for an electret condenser microphone. Insert a 2-kΩ resistance and more than 10 µF electrolytic capacitor in series between this pin and the analog GND.
GPIO0	49	D	I/O	HZ (IN)	GPIO	These are general-purpose I/O ports. The selection of input and output and the output level are set by the control resistor. After resetting, the ports are put in the input mode as a default state. Pull down when not in use.
GPIO1	50	D	I/O	HZ (IN)	GPIO	
GPIO2	51	D	I/O	HZ (IN)	GPIO	
GPIO3	52	D	I/O	HZ (IN)	GPIO	
GPIO4	62	D	I/O	HZ (IN)	GPIO	
GPIO5	63	D	I/O	HZ (IN)	GPIO	
GPIO6	1	D	I/O	HZ (IN)	GPIO	
GPIO7	2	D	I/O	HZ (IN)	GPIO	
GPIO8	3	D	I/O	HZ (IN)	GPIO	
GPIO9	4	D	I/O	HZ (IN)	GPIO	
TEST1	7	D	I	—	ETC	Test pin. Fix to GND.
TEST2	6	D	I	—	ETC	
VREF	25	A	I/O	HZ (OUT)	ETC	This pin is an internal analog reference voltage. Insert an electrolytic capacitor of more than 10µF between this pin and analog GND. The attributes of input and output are determined by resistor setting.

Symbol	Pin No.	A/D/P	I/O	DEF	Group	Description
DVDD1	48	P	—	—	POW	This pin is a digital power supply. Fix to +3.3 V. Insert a 0.1μF laminated ceramic capacitor between this pin and the digital VSS of the same number. Insert the capacitor as close to the pin as possible.
DVDD2	64	P	—	—	POW	
AVDD1	11	P	—	—	POW	This pin is an analog power supply. Fix to +3.3 V. Insert a 0.1μF laminated ceramic capacitor between this pin and the analog VSS of the same number. Insert the capacitor as close to the pin as possible.
AVDD2	18	P	—	—	POW	
AVDD3	27	P	—	—	POW	
AVDD4	32	P	—	—	POW	
AVDD5	46	P	—	—	POW	
DVSS1	54	P	—	—	POW	Connect this pin to the digital GND. The pattern must be designed so that this pin is separated from the analog GND.
DVSS2	8	P	—	—	POW	
AVSS1	16	P	—	—	POW	Connect this pin to the analog GND. The pattern must be designed so that this pin is separated from the digital GND.
AVSS2	23	P	—	—	POW	
AVSS3	30	P	—	—	POW	
AVSS4	35	P	—	—	POW	
AVSS5	41	P	—	—	POW	
CVSS1	10	P	—	—	POW	This is a common GND for the analog and digital sections. Connect this pin to the analog GND.
CVSS2	36	P	—	—	POW	
N.C.	9, 17, 26, 31, 53, 61	—	—	—	—	Non-connection pin. Make is open.

Note: • A/D/P mean an Analog terminal, Digital terminal, and Power terminal.
- DEF means reset state. H/L stand for output levels. Hz means high impedance and IN means input state (high impedance).
- Group categories are as follows:
HOST-Host interface, TSC-Touch screen interface, TEL-Telecom CODE, VB-Voice band CODEC, ETC-The other, POW-power supply.

5. Functional description

5.1 Hardware interface

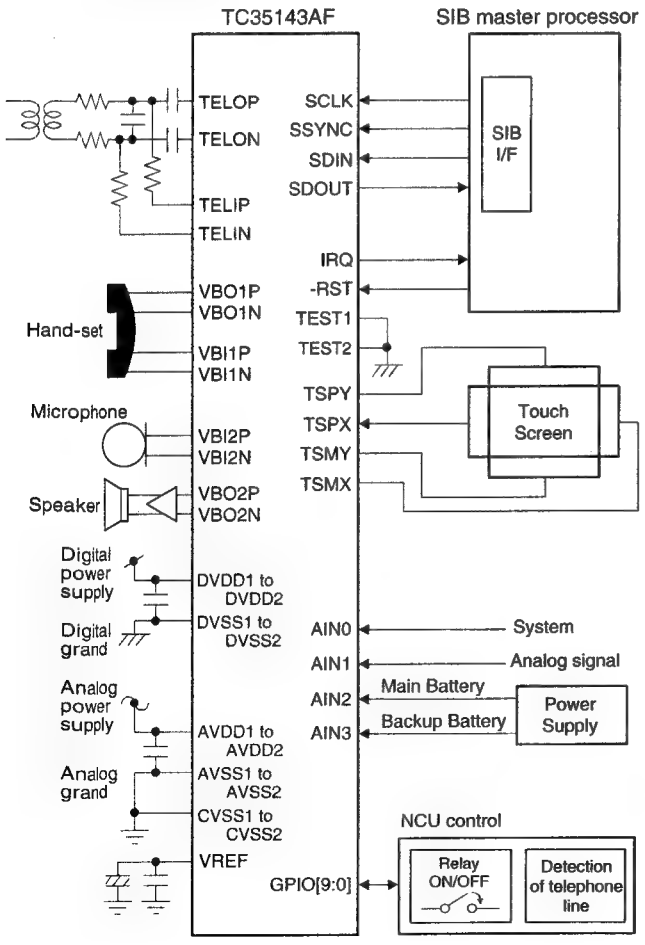


Fig. 5.1.A A typical TC35143AF system configuration

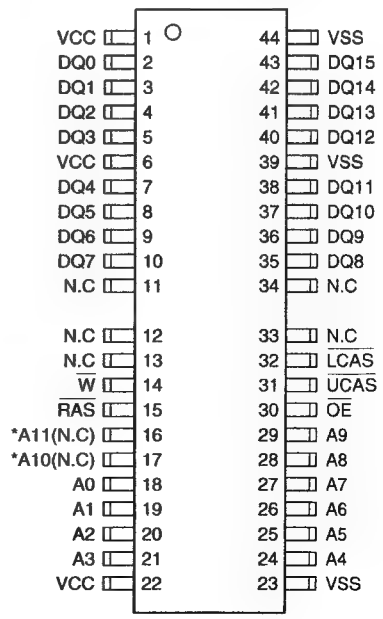
2-3. 16M DRAM

1. DESCRIPTION

This is a family of 1,048,576 × 16 bit Extended Data Out CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage (+5.0V or +3.3V), refresh cycle (1K Ref. or 4K Ref.), access time (-45, -5, or -6), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 1M × 16 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as graphic memory unit for microcomputer, personal computer and portable machines.

2. PIN CONFIGURATION (Top Views)

KM416C/V10(2)04CT



* A10 and A11 are N.C for KM416C/V1204C (5V/3.3V, 1K Ref. product)

T: 400mil 50 (44) TSOP II

Pin Name	Pin Function
A0-A11	Address Inputs (4K Product)
A0-A9	Address Inputs (1K Product)
DQ0-15	Data In/Out
Vss	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
Vcc	Power (+5V)
	Power (+3.3V)
N.C	No Connection

2-4. 4M flash memory

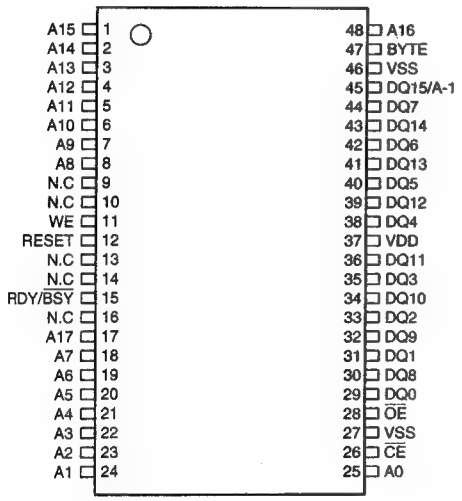
1. General description

TC58FVT400/B400 are 4,194,304-bit (consisting of 524,288 words × 8 bits or 262,144 words × 16 bits) flash memories which are electrically erasable and writable by a 3-V battery. Using the JEDEC standard command control method for the standard E2PROM, they can easily interface with a microprocessor and data can be easily written onto and erased from memory on board. The execution and verification of write and erase are automatically performed inside. Data can be erased in a batch or by block or blocks.

The package is a 44-pin plastic SOP or 48-pin TSOP suitable for high-density, thin-type mounting.

2. Pin connections (TOP VIEW)

TC58FVT400FT/B400FT (TSOP)



3. Pin names

A0 ~ A17	Address input
DQ0 ~ DQ14	Data input and output
DQ15/A-1	Data input and output/address input
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{BYTE}$	Word/byte selection input
$\overline{WE}$	Write enable input
RDY/$\overline{BSY}$	Ready/busy output
$\overline{RESET}$	Hardware reset input
NC	Not connected
V_{DD}	Power supply
V_{SS}	Ground

2-5 Key gate array specifications

1. General description

1) Outputs the electric current dimmer control signals (VR1, VR0)
2) Outputs the duty dimmer control signal (BLCPWN).
3) General-purpose I/O port (10[2:0])
4) Outputs the delay control signal (LPOUT) for A/D conversion start timing.
5) Generates MROM chip selects (MROMCS7B MROMCS2B).
6) Generates FROM chip select (PFROMB).
7) Key control (ROW[7:0], KEYINT)

2. MROM chip select signals

Mask ROM chip select signals are active low signals which are generated by the higher latch address LHAs5 (generated inside), LHA24 (generated inside), address LHA23, and chip select signal CSOB). The output is controlled by the try state control VCC31N and in high impedance when the VCC31N is at low level.

A pullup resistance is required externally. The logical table is as follows:

Select	Capacity	Address	Logic
MROMCS7B	8MB	1F800000 -1FFFFFFF	LHA25=1, LHA24=1, LHA23=1, CSOB=0
MROMCS6B	8MB	1F000000 -1F7FFFFF	LHA25=1, LHA24=1, LHA23=0, CSOB=0
MROMCS5B	8MB	1E800000 -1EFFFFFF	LHA25=1, LHA24=0, LHA23=1, CSOB=0
MROMCS4B	8MB	1E000000 -1E7FFFFF	LHA25=1, LHA24=0, LHA23=0, CSOB=0
MROMCS3B	8MB	1D800000 -1DFFFFFF	LHA25=0, LHA24=1, LHA23=1, CSOB=0
MROMCS2B	8MB	1D000000 -1D7FFFFF	LHA25=0, LHA24=1, LHA23=0, CSOB=0

* LHA25 and LHA24 are address signals (inside) generated by latching HA12 and HA11, respectively, at the rise of ALE. PONB or VCC31N is reset when low.

3. FROM chip select

FROM chip select signals are active low and selected by CS2B (CS1NB) when a mask ROM memory board is mounted and selected by CS0B (CS0B) when not. They are controlled by the try state control signal VCC3IN and in high impedance when the VCC3IN is low. The presence or absence of the memory board is judged by the MBINB. If the MBINB is low, the memory board is mounted and it is high, the memory board is not mounted. The inversion output of MBINB is output as MBINOUT.

4. Key control

When VCC3IN is high and when any bit of the COLUMN [15:0] is high, KEYINT is becomes high.

Address HA[8:1] is latched by ROWSTB (internal signal) generated by a combination of LHA24 (generated inside) and chip select signal KGACSB, and output to ROW [7:0]. Address HA [8:1] is in high impedance when each bit of ROW [7:0] is 0. It also becomes 0 when the VCC3IN is low.

By reading address 60XXXXXXh, COLUMN [15:0] is read into data bus D [15:0].

5. Setting resisters

The duty dimmer (period, duty ratio), A/D conversion start timing delay are general-purpose I/O (Read/Write) are set by setting the following four resisters. Each of the four resisters is readable and writable.

1) Backlight dimmer: 61000000h R/W
2) Periodical resister: 61000004h R/W
3) Reset resister: 61000008h R/W
4) Delay resister: 6100000Ch R/W

5.1 Backlight dimmer

Address: 61000000h R/W VR, TEST, IOWE

bit	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	VR1	VR0	TEST	—	—	IOWE2	IOWE1	IOWE0
Initial value	—	—	—	0	0	0	—	—	0	0	0

VR[1:0]: Controls the output of VR1 and VR0 terminals.
Outputs low when 0 and high when 1.

TEST: The machine gets into the test mode when 1 is written.
Usually set to 0.

IOWE[2:0]: I/O switching bit for general-purpose I/O port 10 [2:0].
Correspond to 102, 101, 100. Input when 0 and output when 1. 10[2:0] needs a pull-down resistance.

* The value currently set is returned when reading.
All bits are 0 when PONB is low.

5.2 Periodic resister

Address: 61000004h R/W EN, BPWF

bit	10	9	8	7	6	5	4	3	2	1	0
	—	—	EN	BPWF7	BPWF6	BPWF5	BPWF4	BPWF3	BPWF2	BPWF1	BPWF0
Initial value	—	—	0	0	0	0	0	0	0	0	0

EN: This is the enable signal which outputs BLCPWN.
No output when EN = 0; output when EN = 1.

BPWN[7:0]: The period of BLCPWN is set by writing 00h ~ FFh.
The range can be set 993 Hz (1007 µs) to 113.8 Hz (8.79 ms), by writing 00h and FFh, respectively.
Frequency Fd = BC32K/(BPWF+33)
Period T = 1/Fd

* The value currently set is returned when reading.
All bits become 0 when PONB or VCC3IN is low.

5.3 Reset resister

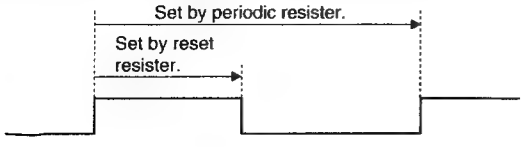
Address: 61000008h R/W BPDF

bit	10	9	8	7	6	5	4	3	2	1	0
	—	—	BPDF8	BPDF7	BPDF6	BPDF5	BPDF4	BPDF3	BPDF2	BPDF1	BPDF0
Initial value	—	—	0	0	0	0	0	0	0	0	0

BPDF[8:0]: Sets the high period width of the BLCPWN signal.
Always outputs low by writing 000h.
Always outputs high by writing 1FFh.

* The value currently set is returned when reading.
All bits become 0 when PONB or VCC3IN is low.

The relationship between the period and duty ratio is shown below. For the setting of each resister, see the attached data.



5.4 Delay resister

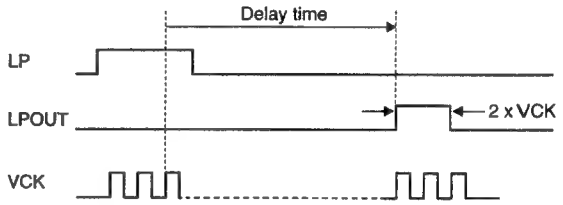
Address: 6100000Ch R/W IOB, LPDLY

bit	10	9	8	7	6	5	4	3	2	1	0
	IOB2	IOB1	IOB0	LPDLY7	LPDLY6	LPDLY5	LPDLY4	LPDLY3	LPDLY2	LPDLY1	LPDLY0
Initial value	0	0	0	0	0	0	0	0	0	0	0

IOB [2:0]: I/O port output bit
Outputs low when 0 and high when 1.

LPDLY [7:0]: Sets the delay time of LP delay signal LPOUT by writing 00h FFh.
Delay time Td = (256 LPDLY).VCK.
The pulse width of LPOUT is 2 × VCK.

* The value currently set is returned when reading.
All bits become 0 when PONB is 0.



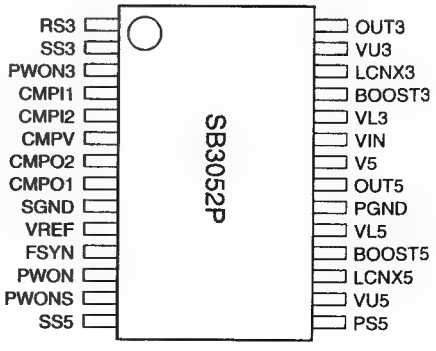
2-6 DUAL CHANNEL STEP DOWN DC-DC CONVERTER CONTROLLER SB3052P

Features

- 5V/3.3V (internally fixed), dual output step-down DC-DC converter controller
- High load follow-up by current control PWN method.
- High-efficiency conversion (95%) by synchronous commutation. High efficiency is maintained by lowering the frequency under light loads.
- External power MOSs are all Nch-MOSFET.
- Maximum Duty width is 92% (300 kHz).
- PWM frequency can be selected between 200 KHz/300 kHz. Possible to synchronize with external oscillator.
- Shut-down and stand-by functions, overcurrent protection (drooping type), soft start function.
- Two high-performance comparators are incorporated. Suitable for generating the output voltage power good signal.

Pin configuration diagram

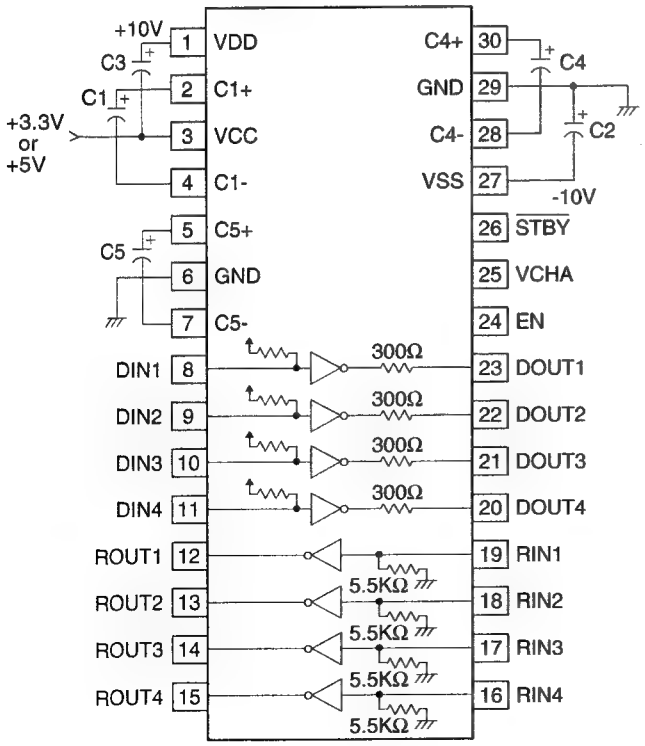
SSOP-28P PACKAGE



No.	Symbol	Description
1	RS3	3.3 V current comparator (+) input
2	SS3	3.3 V soft start time setting
3	PWON3	3.3 V ON/OFF input
4	CMPI1	Comparator 1 non-inversion input
5	CMPI2	Comparator 2 non-inversion input
6	CMPV	Comparator 1&2 positive power supply input
7	CMPO2	Comparator 2 output
8	CMPO1	Comparator 1 output
9	SGND	Small signal ground
10	VREF	3.3V reference voltage output
11	FSYN	Internal oscillator frequency setting/external synchronizing signal input
12	PWON	Power-on signal input (LOW=Shutdown)
13	PWON5	5.0 V ON/OFF input
14	SS5	5.0V soft start time setting
15	RS5	5.0V current comparator (+) input
16	VU5	5.0V upper arm power NMOSFET drive
17	LCNX5	5.0V switching node
18	BOOST5	5.0V upper arm power NMOSFET driving power supply input
19	VL5	5.0V lower arm power NMOSFET drive
20	PGND	Power ground
21	OUT5	5.0V voltage detection/current comparator (–) input
22	V5	Internal 5V power supply output
23	VIN	Power supply input
24	VL3	3.3V lower arm power NMOSFET drive
25	BOOST3	3.3V upper arm power NMOSFET driving power supply input
26	LCNX3	3.3V switching node
27	VU3	3.3V upper arm power NMOSFET drive
28	OUT3	3.3V voltage detection/current comparator (–) input

2-7 RS-232C line driver/receiver

Block diagram/terminal connection diagram (top view)



Note 1: VDD and VSS are terminals from which internally boosted voltage is output. Do not connect loads directly to this terminal.

Note 2: It is recommended use capacitors C1 C5 with a voltage resistance of more than 20V. Insert a bypass capacitor of 0.1 - 1 µF between VCC and GND.

Note 3: When used with VCHA = L (5V mode), it is not necessary to connect the C5 capacitor. Keep pins 5 and 7 open.

Note 4: The pull-up resistance for driver input is an active resistance.

Logical value table

Driver

$\overline{STBY}$	DIN	DOUT	Remarks
L	X	Z	Stand-by mode (D/D conversion stopped)
H	L	H	Space level output
H	H	L	Mark level output

Receiver

$\overline{STBY}$	EN	RIN		ROUT		Remarks
		R3 ~ R4	R1 ~ R2	R3 ~ R4	R1 ~ R2	
L	L	X	X	H	H	Stand-by mode 1 (D/D conversion stopped)
L	H	L	X	H	H	Stand-by mode 2 (D/D conversion stopped, R3 ~ R4 in action)
L	H	H	X	L	H	Stand-by mode 2 (D/D conversion stopped, R3 ~ R4 in action)
H	X	L		H		Mark level input
H	X	H		L		Space level input

Switching between 3V and 5V (Note 14)

VCHA	Operation mode
L	5V mode (dual boosting)3V mode
H	3V mode (triple boosting)

H: High level, L: Low level, Z: High impedance, X:H or L

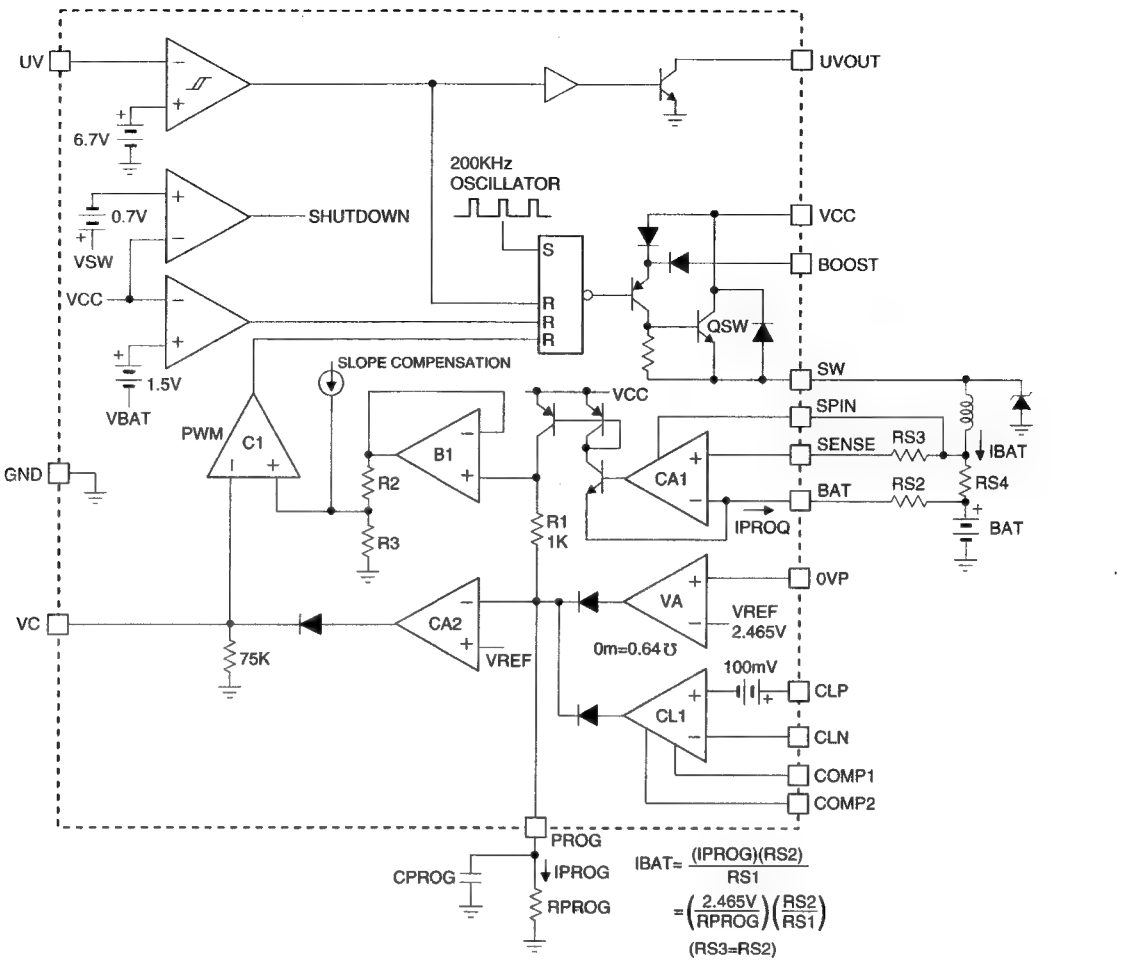
Note1: The switching of the VCHA terminal must be performed in the stand-by mode ($\overline{STBY}$=L).

2-8 Constant-current, constant-voltage battery charger with input current limit (LT1511)

Features

- Simple design for charging NiCd, NiMH, and lithium rechargeable batteries the charge current is programmable by a resistance or DAC.
- The adapter current loop tolerates the maximum charge current when the computer is being used.
- An accuracy of 0.5% is obtained in the voltage mode charge.
- High efficiency by 4A built-in switch, current mode PWN.
- 5% charge current accuracy
- Variable low-voltage lockout
- Power is automatically shut down when AC adapter is removed.
- Low battery current consumption: 3 µA
- Current can be sensed by either battery terminal.
- Charge current soft start
- Shutdown control

2. Block diagram.



3. Pin description

GND (Pins 1, 4, 5, 7, 16, 23, 24): Ground pin

SW (Pin 2): Switch output. A short key catch diode must be installed close to the SW pin and GND, by using a short lead.

Vcc (pins 20, 21, 22): Chip power supply. For proper bypassing, it is required to have a low ESR capacitor of more than 20 µF with the shortest lead. VCC must be at least 3V higher than VBAT within the range of 8V to 28V. When VCC drops below 7V, low-voltage lock starts, stopping switching operation. Note that there is a parasitic diode between SW pin and VCC pin. When the battery is used, VCC must not be lower than 0.7 V from SW. Short 3 VCC pins in group.

BOOST (pin 3): This pin is a low ON voltage and consumes less power, and thus is used for boost trapping and driving the switch power NPN transistor. Under normal operation, VBOOST = VCC + VBAT. The maximum allowable VBOOST is 55 V.

SENSE (pin 12): It is possible to sense by either of the current amplifier CA1 input and battery.

BAT (pin 14): Current amplifier CA1 input.

SPIN (pin 13): This pin is used for the internal amplifier CA1 bias. It is required to connect to RS1, as shown in the 3A lithium battery charger circuit (Fig. 1).

PROG (pin 19): This pin is used for charge current programming and system loop compensation. During normal operation, VPROG is maintained at around 2.465V. When shorted to GND, switching is discontinued. When programming the charge current using the microprocessor control DAC, the current must be synchronized following up maximum 2.465V.

Vc (pin 18): This is the internal loop control signal for the current mode PWM. Switching is started at 0.7V. Higher the VC value, the higher the charge current during the normal operation. When a capacitor of more than 0.33 µF is connected to GND, noise is filtered to control soft start speed. Switching is stopped by pulling down this pin to L. The standard output current is 30 µA.

OVP (pin 8): This in an input to amplifier VA which has 2.465V threshold. The standard input current is about 3nA. To charge the lithium-ion battery, the VA monitors the battery voltage and reduces the charge voltage when the battery voltage reaches the preset value. The OVP pin must be grounded when not used.

UV (pin 6): Low-voltage lockout input. Threshold at the rise is 6.7V, with 0.5V hysteresis. Switching is stopped by low-voltage lockout. When power supply (usually wall adapter output) to the chip is stopped, UV pin must be pulled down below 0.7 V (a resistance of 5K is needed between adapter output and ground). Otherwise, the reverse battery current passing through the chip becomes about 200 µA, instead of 3µA. UV pin must not be in float state. If the UV pin is connected to VIN without using voltage dividing circuit, the internal 6.7V low-voltage lockout is started.

UVVOUT (pin 17): This is a low-voltage lockout status open collector output. In low voltage state, this pin is in L state. When an external pull-up resistance is connected, an active VCC becomes H. Even when VIN is removed, UVOUT is kept in L, and the pull-up current must be kept at less than 100 µA.

CLP (pin 9): This is a positive input to the power supply current limit amplifier CL1. The threshold is set to 100mV. When using for limiting the power supply current, a filter which filters 200 kHz switching noise is needed.

CLN (pin 10): This is a negative input to the amplifier CL1 and connected to VCC. To reduce noise further, connect to VCC bypass capacitor.

COMP1 (pin 11): This is an amplifier CL1 compensation node. When using the input current amplifier CL1, a capacitor of 200 pF is needed between this pin and ground. When input adapter current is limited, this node increases to 1V. When the COMP1 is forcefully made to L by the external transistor, the amplifier CL1 becomes inoperative. (Adapter current limit is removed.) COMP1 can source 200 µA.

COMP2 (pin 15): This is also an amplifier CL1 compensation node. Its voltage is up to 2.8 V when input adapter current is limited or when constant-voltage charge is performed.

2-9. PCMCIA control ER (TC6345AF)

1) GENERAL DESCRIPTION

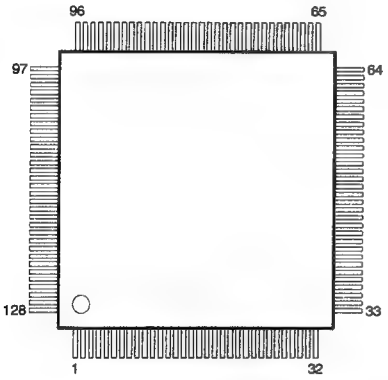
The TC6345AF is a small footprint ASIC intended for use with Personal Information communicators, that are based on the TMPR3905/12.

The TC6345AF provides full level-shifting and isolation buffers for a single 3.3V or 5V PCMCIA socket, including address and data busses, as well as PCMCIA control and status signals.

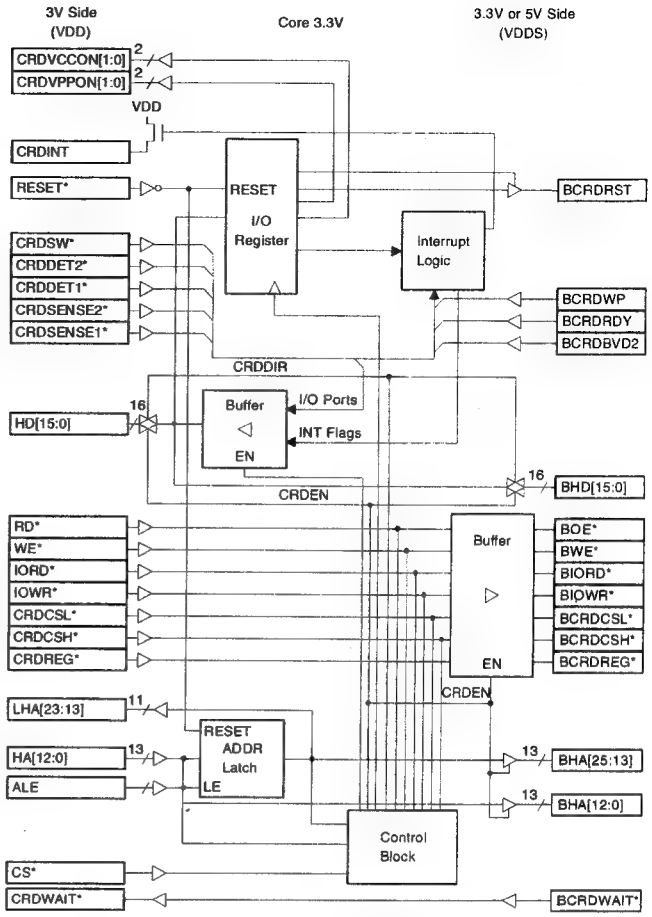
2) FEATURES

- Replaces discrete buffers with a single TC6345AF chip per PCMCLA socket
- Full level-shifting and buffering for 3.3V and 5V sockets.
- Supports PCMCIA control/status signals, minimizing system impact to the TMPR3905/12 general purpose I/O pins.
- Sensing of card operating voltage for future 3.3V cards
- Provides control registers and pins for generating on/off control signals for switchable card VCC and VPP power supplies
- Includes system address latch, which is needed to generate the upper address bits for ROM, SRAM and Flash
- 128-pin LQFP package (14mm × 14mm body, 0.4mm pin pitch)

3) PACKAGE DIMENSION



4) BLOCK DIAGRAM



Note: This figure illustrates I/O pins configured in a typical PCMCIA arrangement. Some pins can be configured in other ways.

5) PIN ASSIGNMENT

NO.	I/O	SIGNAL NAME
1	—	VSS
2	O	BHA [4]
3	I/O	BCRDRST
4	O	BHA [5]
5	I/O	CRDSENSE2*
6	O	BHA [6]
7	O	BHA [25]
8	O	BHA [7]
9	O	BHA [24]
10	O	BHA [12]
11	—	VDDS
12	O	BHA [23]
13	O	BHA [15]
14	O	BHA [22]
15	O	BHA [16]
16	O	BHA [21]
17	I/O	BCRDRDY
18	O	BHA [20]
19	O	BWE*
20	O	BHA [19]
21	O	BHA [14]
22	—	VDDS
23	O	BHA [18]
24	O	BHA [13]
25	O	BHA [17]
26	O	BHA [8]

NO.	I/O	SIGNAL NAME
27	O	BIOWR*
28	O	BHA [9]
29	O	BIORD*
30	O	BHA [11]
31	I/O	CRDSENSE1*
32	—	VSS
33	—	VDDS
34	O	BOE*
35	O	BCRDCSH*
36	O	BHA [10]
37	I/O	BHD [7]
38	O	BCRDCSL*
39	I/O	BHD [6]
40	I/O	BHD [15]
41	I/O	BHD [5]
42	I/O	BHD [14]
43	I/O	BHD [4]
44	I/O	BHD [13]
45	I/O	BHD [3]
46	I/O	BHD [12]
47	I/O	CRDDET1*
48	I/O	BHD [11]
49	—	VSS
50	I/O	CRDSW*
51	I/O	LHA [23]
52	I/O	LHA [22]

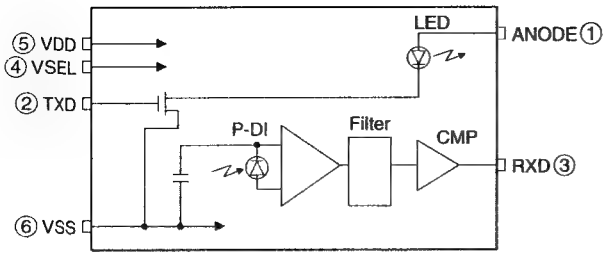
NO.	I/O	SIGNAL NAME
53	I/O	LHA [21]
54	I/O	LHA [13]
55	I/O	LHA [14]
56	I/O	LHA [15]
57	I/O	LHA [16]
58	I/O	LHA [17]
59	I/O	LHA [18]
60	I/O	LHA [19]
61	I/O	LHA [20]
62	I/O	CRDVPPON [0]
63	I/O	CRDVPPON [1]
64	—	VDD
65	—	VSS
66	I/O	CRDVCCON [0]
67	I/O	CRDVCCON [1]
68	I	RESET*
69	I	HA [0]
70	I	HA [1]
71	I	HA [2]
72	I	HA [3]
73	I	HA [4]
74	I	HA [5]
75	I	HA [6]
76	I	HA [7]
77	I	HA [8]
78	I	HA [9]

NO.	I/O	SIGNAL NAME
79	I	HA [10]
80	I	HA [11]
81	—	VDD
82	I	HA [12]
83	O	CRDINT
84	I	IORD*
85	I	IOWR*
86	I	CRDREG*
87	O	CRDWAIT*
88	I	CRDCSL*
89	I	CRDCSH*
90	I	CS*
91	I	WE*
92	I	ALE
93	I	RD*
94	I/O	HD [0]
95	I/O	HD [1]
96	—	VSS
97	—	VDD
98	I/O	HD [2]
99	I/O	HD [3]
100	I/O	HD [4]
101	I/O	HD [5]
102	I/O	HD [6]
103	I/O	HD [7]
104	I/O	HD [8]

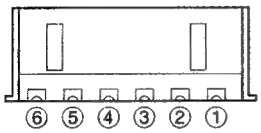
NO.	I/O	SIGNAL NAME
105	I/O	HD [9]
106	I/O	HD [10]
107	I/O	HD [11]
108	I/O	HD [12]
109	I/O	HD [13]
110	I/O	HD [14]
111	I/O	HD [15]
112	—	VSS
113	I/O	CRDDET2*
114	I/O	BCRDWP
115	I/O	BHD [2]
116	I/O	BHD [10]
117	I/O	BHD [1]
118	I/O	BHD [9]
119	I/O	BHD [0]
120	I/O	BHD [8]
121	O	BHA [0]
122	I/O	BCRDBVD2
123	O	BHA [0]
124	O	BCRDREG*
125	O	BHA [2]
126	O	BHA [3]
127	I	BCRDWAIT*
128	—	VDDS

2-10. IR MODULE

1) Block Diagram



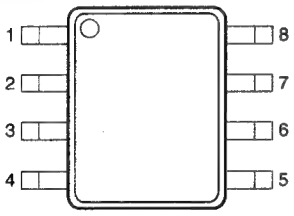
2) Pin Configuration



① ANODE ④ VSEL
② TXD ⑤ VDD
③ RXD ⑥ VSS

2-11. Elevating Voltage DC-DC Converter (SB2020P)

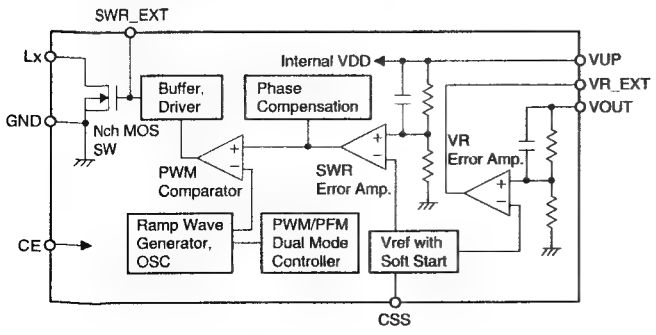
1) Pin Assignment and Function



SOP-8 package

Pin	Symbol	Function
1	GND	Ground pin
2	VOUT	Regulator output pin
3	VR_EXT	PNP transistor drive pin
4	CSS	Software start capacitor connect pin
5	VUP	SWR output/power pin
6	CE	Chip enable pin
7	SWR_EXT	SWR external transistor drive pin (CMOS output)
8	Lx	SWR switch pin

2) Block Diagram



2-12. LCD contrast control

The display contrast of this unit is D-A converted by the general-purpose port of the LCD controller and supplied to the VCON terminal of the LCD unit.

D-A conversion is performed in 256 stages by 8 bits of each of VR1 to VR8 allocated to the LCD controller general-purpose port.

The optimal value of contrast is factory set and stored in the 4MB flash memory.

Therefore, whenever the 4MB flash memory ore PWB unit is replaced, the contrast needs to be set again.

Here is the procedure for setting the contrast.

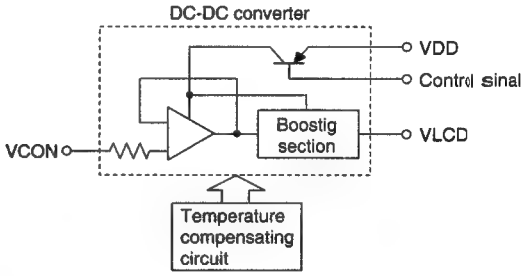
[Setting procedure]

No	Operating procedure	Display	Check item
1	Enter the Normal diag mode with "2" + "W" + RESET	Diag menu	
2	Select 2. SET contrast with the tablet and press Enter.		
3	Adjust the contrast with - key so that the four lines at the center of the screen are clear and uniform in thickness.		
4	Press [CTRL] + [W] to store the contrast value in memory.		Set Flash : *** ...OK Check the display of OK.
5	Press [POWER] to return to the Menu.		

LCD Vcon terminal configuration

The potential of the contrast control terminal Vcon is converted into the LCD driving voltag 20e (VLCD) by the circuit shown in Figure 1, which is incorporated in the LCD unit.

The LCD driving voltage (VLCD) is automatically adjusted according to the ambient temperature by the temperature compensating circuit.



2-13. State of battery charge

1) State of battery charge of main battery

This unit shows the state of battery charge o 20f the main battery in the following three ways.

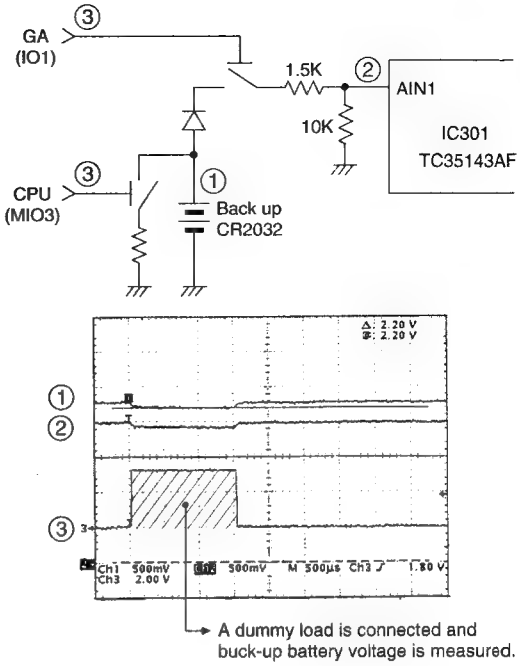
The state of battery charge is sensed by the BMU (battery management unit) of the battery pack and data is sent to the CPU.

Residual voltage capacity	Displayed by○S
about 100 – 20%	GOOD
about 20 – 7.5%	LOW
below 7.5%	VERY LOW

2) State of battery charge of back-up battery

This unit shows the state of battery charge of the back-up battery in the following three ways.
The state of battery charge is measured by the AD converter of ANALOG ASIC (TC3514 203AF) and displayed as shown below.
The voltage of the back-up battery is measured with a dummy load applied to the battery.
The dummy load is controlled by the 101 of GA (SC12307-0J).

Residual voltage capacity	Displayed by OS
about 2.4 V	GOOD
about 2.4 – 2.1 V	LOW
below about 2.1 V	VERY LOW



2-14. Description of the PV5000 power supply circuit

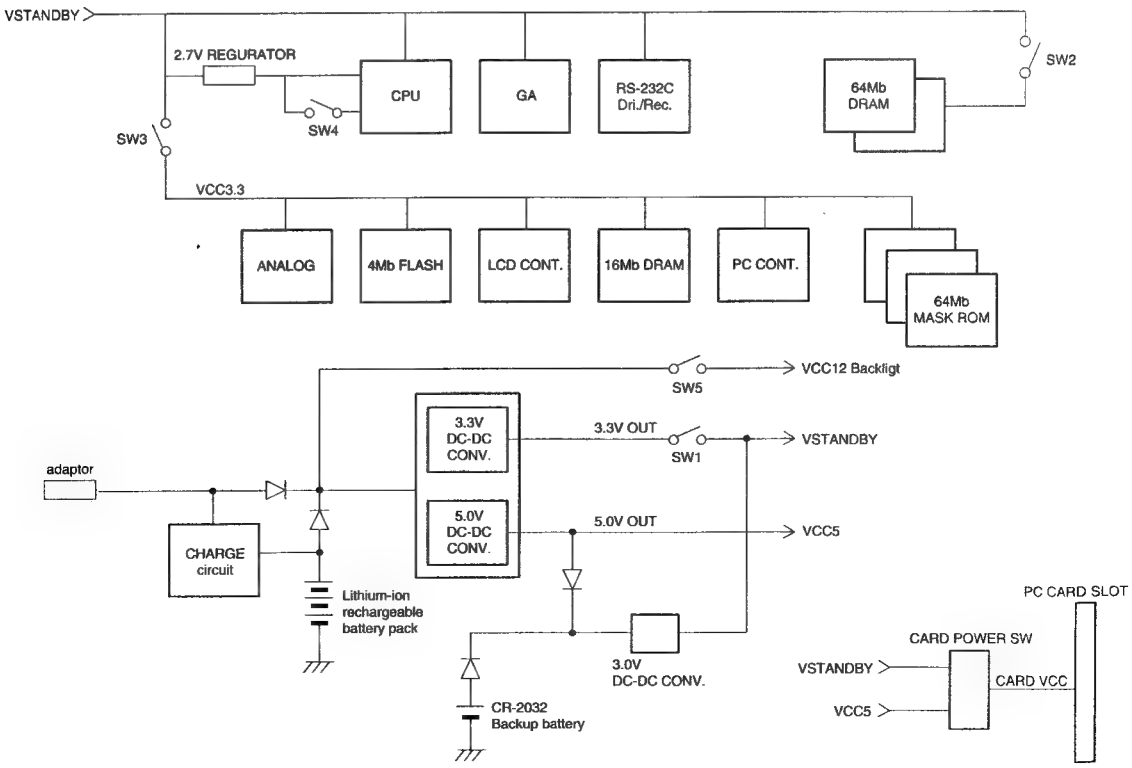
For the power supply, see the power supply circuit diagram.

1) The SW1 alone turns on when the user removes the power supply starting rubber or when the AD adapter is connected to the PC.
2) The SW2 - SW5 turn on when the user presses the [POWER] key.
3) After step 2, the SW2 remains on except when the following conditions are satisfied.
   (1) The main battery and back-up battery discharged completely and the AC adapter is not connected.
   (2) The user pressed the full reset switch.
4) After step 2), the SW3 - SW5 remain OFF when the unit is off and ON when the unit is on.
5) The back-up battery retains the CPU/GA/RS232C 64MB DRAM connected to VSTANDBY.

The switches are controlled by the following signals:

SW1: Turns on and off by the main battery or the AC adapter. (Turns on when there is a voltage on VCC5.)
SW2: CPU's M1026 (DRAMVCCON)
SW3: CPU's PWRCS
SW4: CPU's PWRCS
SW5: CPU's M106 (BLVCCON)

PV-5000 Power supply circuit



2-15. Lithium-ion secondary battery

1. Major functions of battery pack

Here are some of the major functions of the battery pack and the related characteristics of the PC.

- The battery management unit (BMU) manages the residual capacity of the battery block in the unit of ampere hour. The quantity of electricity measured in Ah is converted by internal arithmetic operation of the BMU into the quantity of energy measured in Wh.
- To improve the safety of operation, overcharge (overvoltage) control [both voltage detection and charge current shut-off] is duplicated at the component level. As the primary stage of control, the voltage of each battery cell is individually monitored by the microprocessor. If the voltage of any cell exceeds the specified value, the charge FET turns off to shut off the charge current. As the secondary stage of protection, the voltage of each battery cell is individually detected by the special voltage sensing IC. If the voltage of any cell exceeds the specified value, the non-resettable thermal fuse (with resistance) is blown out to shut off the charge current.
- P-ch FET is used for both charge and discharge control.

  If the thermal fuse (with resistance) is blown out by the microprocessor or the special voltage sensing IC due to the occurrence of any abnormal condition, or if the battery voltage is lower than the reset voltage of the regulator, the BMU operates on the power supplied by the charger of the PC, making it possible to communicate with the PC.
- If the voltage of any battery cell is lower than the specified minimum value, the battery is recharged at a low rate through the trycle charge circuit inside the BMU. After that, when the voltage of the cell which has showed the minimum voltage becomes higher than the specified value, the quick charge circuit is turned on and the trycle charge circuit is turned off, and thus quick charge is started.
- If the voltage of the battery cell which shows the lowest voltage is higher than the specified value, the battery is recharged by the specified voltage and current (CV/CC: constant voltage/constant current) supplied from the PC's charger.
- Charge temperature control, such as permitting or prohibiting charging, and suspending charging process due to increase or drop in battery cell temperature during charging, is carried out by the BMU.
- Charge termination is controlled by the BMU. When requirements for terminating charging are satisfied, the BMU carries out the charge-complete operation. At this time, the BMU makes the relative residual capacity at 100% and sets the learned capacity to the absolute residual capacity. In addition, it turns off the FET and shuts off the charge current supplied from the charger.
- The microprocessor on the BMU is shifted from the sleep mode (low-speed clock operation) to the active mode (high-speed clock operation) when: (1) the installation of the AC adapter is detected (voltage output from CV/CC circuit on the PC); (2) a request for communication from the PC; or (3) the charge or discharge current is higher than 50 mA. The microprocessor on the BMU is shifted from the active mode to the sleep mode when the adapter is not connected (no voltage output from the CV/CC circuit on the PC), the charge or discharge current is lower than 50 mA and no communication is present for 30 seconds.
- In communications, the PC works as the master and the battery pack as the slave. The BMU sends the data corresponding to the command that is sent by the PC synchronizing with the clock the PC generates, to the PC synchronizing with the clock the PC generates following the transmission of the command.
- The communication system is the two-wire, half duplex, bi-directional type.
- The PWROK signal changes from Hi into Lo when the relative residual capacity becomes 6% during discharging or in the stand-by mode. It also becomes Lo regardless of the relative residual capacity in some error modes described later. In addition, if the DETECT signal is Lo, the PWORK signal becomes Lo regardless of the state of battery charge and BMU. Regardless of the relative residual capacity and the voltage of each cell, the PWORK signal changes from Lo to Hi when an AC adapter is detected with the DETECT signal at Hi, or when some errors are overridden with the relative residual capacity being greater than 6% and the DETECT signal at Hi. Table 1 shows the relationship between the PWROK signal and the switching condition of the signal.

  (When the PWROK signal becomes Lo, the PC gets in "Shut-down" mode.

Table 1 Definition of PWROK signals

DETECT	ADP	Relative residual capacity	Discharge/ overcurrent error Charge FET error BMU error Cell balance error	Overdis-ch argeerror	PWROK
Lo	—	—	—	—	Lo
—	None	6%≧	—	—	Lo
—	None	—	—	Occurred	Lo
—	—	—	Any of errors	—	Lo
Other than above					Hi

- The BMU controls the charge/discharge FET using the DETECT signal sent from the PC.When the DETECT signal is Lo (the PC switch is closed), the charge/discharge FET is forcefully turned OFF and PWROK signal is forcefully made into Lo.

  In addition, when the DETECT signal is at Hi (the PC switch is open), the forcefully-off state of the charge/overcharge FET is released to make both the charge/discharge FET and the PWROK signal to the state corresponding to the state of the battery charge.

  Besides, the DETECT signal generating switch and the BMU microprocessor port are connected as shown in Figure 1, and it is pulled up at the BMU side by the 220 kW resistance. Table 2 shows the relationship between the DETECT signal level and the PC operation.

Table 2 Definition of DETECT signals

DETECT signal	Operation
Lo	Charge/discharge FET is forcefully turned OFF and PWROK signal becomes Lo.
Hi	The forcefully-off state of charge/discharge FET is released to make both the charge/discharge FET and the PWROK signal into the state that reflects the state of battery charge.

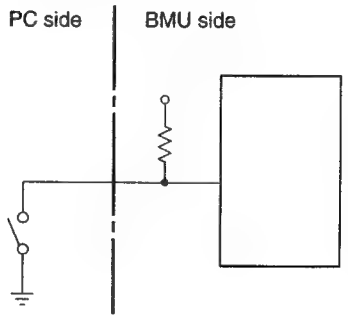


Fig. 1 DETECT signal interface

- When the DETECT terminal is at Hi level, the charge/discharge FET is normally in ON state unless an error (overcurrent, overdischarge, overcharge) occurs.
- For the microprocessor, the data communication task has the top priority. (The data communication interrupt is preferentially carried out even during the calculation of the residual capacity that is performed at periodic intervals.9
- The BMU can recognize the installation of the AC adapter, by sensing the output voltage sent from the CV/CC circuit inside the PC.

2. BMU block diagram

Figure 2 shows the block diagram of the BMU.

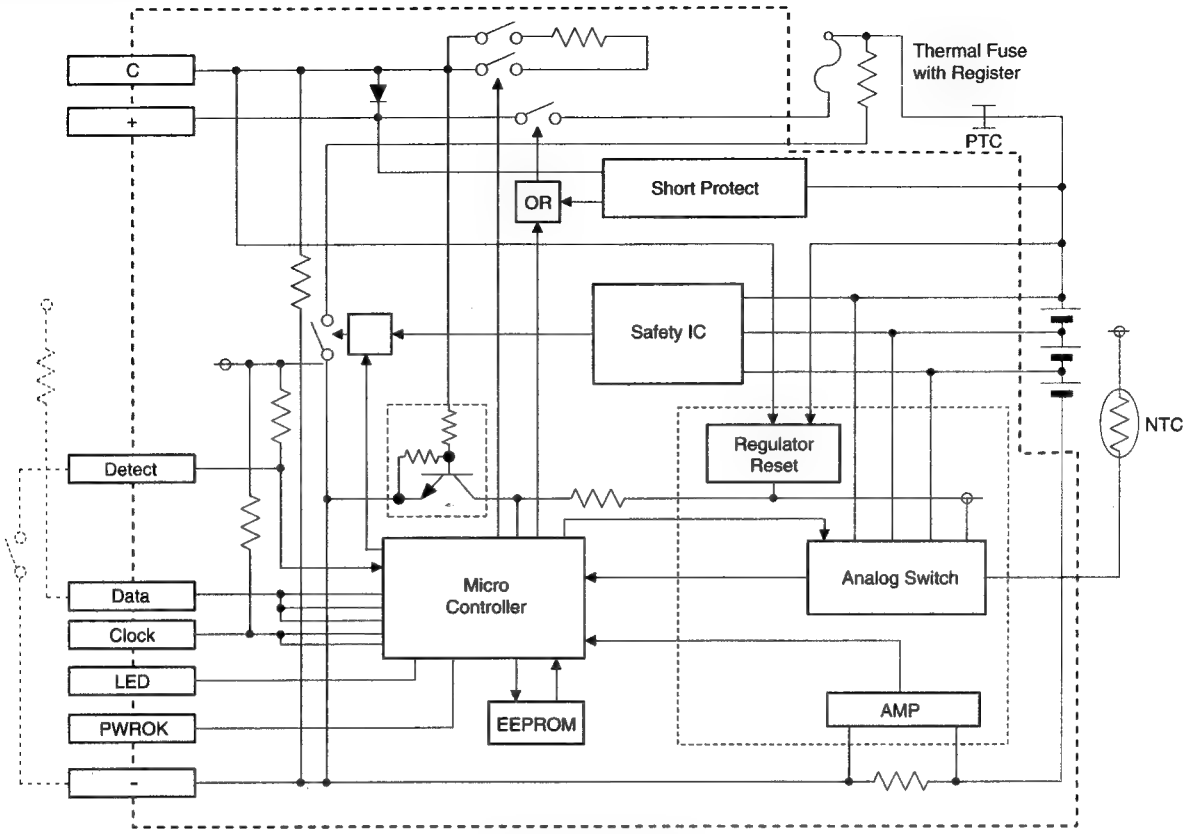


Fig. BMU block diagram

Remarks 1. The following components are located outside the BMU (on the relay PWB inside the battery unit) and connected to it.
1) Thermister
2) PTC

3. LED function

The BMU supplies the signal that drives the LED on the PC according to the battery pack.

- During charge (including trycle charge):
  Light blinks (ON for 1 sec and OFF for 0.5 sec)
- Charge complete:
  Light comes on when the completion of charge is detected, the relative residual capacity is more than 95% and less than 100%, and the adapter is inserted.
- During discharge (w/o AD adapter. Including OFF state):
  OFF
- When an error occurs:
  Light blinks (ON for 0.125 sec and OFF for 0.125 sec)
  When the error is removed, the LED goes out.

Figure 3 shows the connection diagram of the BMU microprocessor port and LED drive device of the PC.

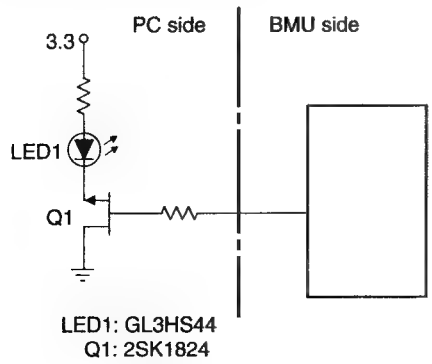
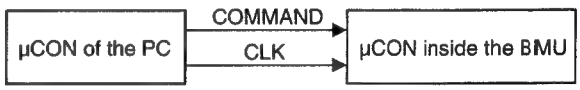


Fig. 3 LED signal connection diagram

Step 1. The PC requests the BMU to send data.



Step 2. The PC receives data from the BMU.

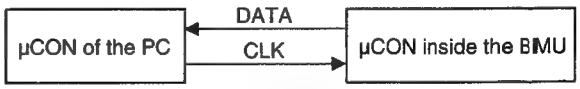


Fig. 5 Communication sequence

4. Interface block diagram

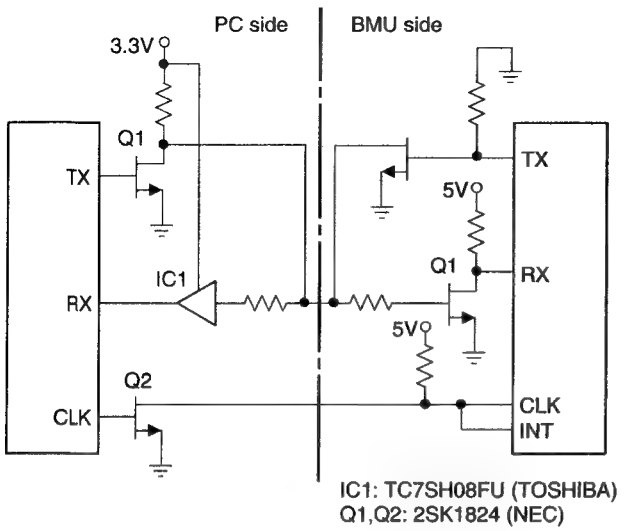


Fig. 6 Interface diagram

5. Power-management control

The following four operation modes are specified for the operation of the BMU.

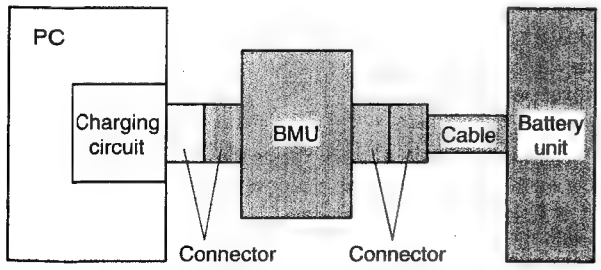
6. I/O terminal

Table 10 shows the I/O terminals for the battery pack.

Table 10 I/O terminal

Pin #	Name	I/O (BMU standards)	Description
1,2,3	CHG	—	Charge
4	DETECT	I	Battery pack insertion detection
5	DATA	I/O	Communication
6	LED	O	Display of state of battery charge
7,8,14,15	—	—	GND
9,10,11	+	—	Discharge
12	PWROK	O	Residual state of charge
13	CLOCK	I	Communication clock

System block diagram



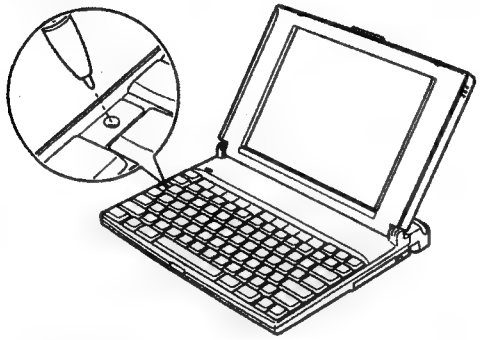
CHAPTER 3. NOTES FOR SERVICING

1. Resetting the device

If the device stops responding while you are using it, you can reset the device. Make sure the device is turned on, and then press the **RESET** button with the stylus.

Caution:

The reset function will not work if the device is turned off when you press the **RESET** button.



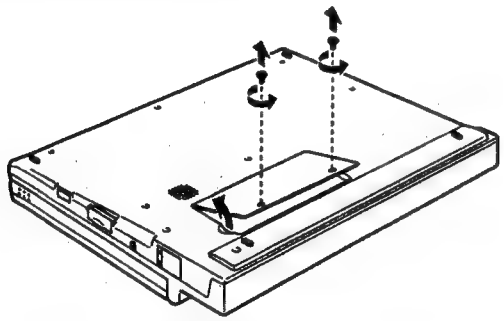
If the problem still persists after you have reset the device, try the following (full reset) remedy.

Full Reset

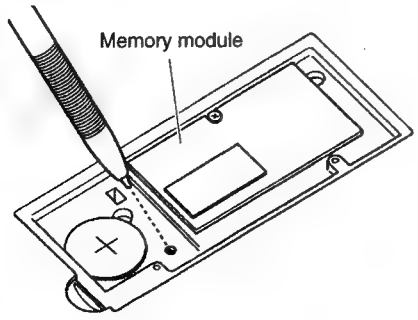
Caution:

The following procedure will cause all data on the device to be lost. Please perform a full back-up prior to this procedure.

1. Turn off the device.
2. Using the provided screwdriver, loosen the two backup battery cover screws on the bottom of the device and remove the backup battery cover.



3. Using the stylus, press the **FULL RESET** button.



Caution:

Do not touch the memory module. Static discharge can destroy it.

4. Replace the memory module cover and fasten it with the two memory module cover screws.
5. Turn on and re-setup the device using the H/PC Setup Wizard.
6. Restore your data from a backup.

Note:

If you forget your password, you must set up your device again, using the above steps.

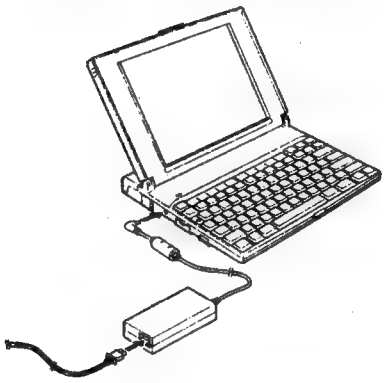
2. Charging the battery pack

When the main battery is low, your device displays warning messages prompting you to change the main battery as soon as possible. You can also check the battery power by double-tapping the power status icon if it appears on the taskbar.

Caution:

Please charge the main battery promptly after the charge becomes low.
Leaving it uncharged for an extended period of time will result in rapid depletion of the data backup battery, and possible loss of all data.

1. Turn off the device.
2. Connect the AC adaptor cable into device's External power port.
3. Connect the AC power cord into AC adaptor.
4. Plug the AC power code into a wall outlet.
   In 2 or 3 seconds after connecting, the charging lamp begins flashing and charging the main battery has started.



Caution:

Always use the AC adaptor (EA-J01V) included with the device. Using other AC adaptors may damage the device.

Note:

The charge lamp lights when the battery is already fully charged.

5. Charging takes about 2 hours and 30 minutes when main battery is almost completely discharged. When the charging lamp lights steadily the main battery is fully charged.
6. Disconnect the AC power cord from the AC outlet and disconnect the AC adaptor from the device.

Note:

Always hold the AC power cord by its plug when removing if from the wall outlet.
Never pull on the cord.

Note:

- The built-in main battery cannot be charged under extremely hot or cold conditions. Under such conditions, the charging lamp stays off. if this occurs, move the device to a location where the temperature is normal, then reconnect the AC adaptor. Charging also stops if the temperature becomes extremely hot or cold while charging is in progress.
- Rapid flashing of the charging lamp (4 times per second) indicates a malfunction. If this occurs, please contact your Sharp dealer.

About power source

- **Caution:** When the main battery is depleted, recharge it promptly. If the depleted main battery is not recharge, the backup battery will be drained more quickly than normal.
- The device will turn off if you ignore the low battery warning and continure to work. If this happens, the data being edited and other information may be lost, and the alarm may not function correctly.

- When you use the AC adaptor, a slight humming noise may be heard. This is normal.
- After charging or prolonged use of the built-in main battery, it may become warm. This is normal, and does not indicate any problem.

Caution:

- The socket outlet must be located near the equipment and be easily accessible.
- When the AC adaptor is not in use, keep it disconnected from a AC outlet.
- Do not use the AC adaptor to operate other equipment, as the equipment may be damaged.
- Avoid using the AC adaptor during an electrical storm.
  Electric shock and damage to the unit from lightning is possible.
- If any fluid which has leaked from the battery enters your eyes rinse them thoroughly with water and seek medical attention immediately, or serious injury could results.

WARNING

THE VOLTAGE APPLIED MUST BE THE SAME AS SPECIFIED ON THE ADAPTOR. USING THE ADAPTOR AT A HIGHER THAN SPECIFIED VOLTAGE IS DANGEROUS AND MAY RESULT IN A FIRE OR OTHER TYPE OF ACCIDENT, THUS DAMAGING THE ADAPTOR. SHARP TAKES NO RESPONSIBILITY FOR ANY DAMAGE RESULTING FROM USE THE ADAPTOR AT VOLTAGES OTHER THAN THAT SPECIFIED.

The capacity of the built-in main battery gradually decreases with repeated use (the deterioration rate depends on the operating temperature and environment). When battery capacity becomes extremely low even after fully charging, you should replace the built-in main battery. Please contact your Sharp dealer.

Caution:

Main battery replacement should be done only by a qyalified service person.
Never attempt to replace the built-in main battery by yourself.

Replacing the backup battery

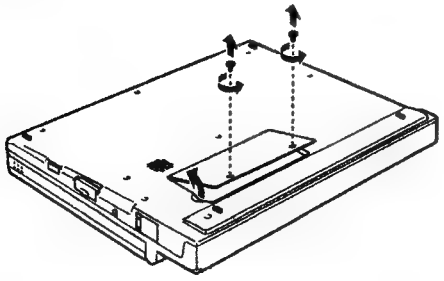
When the backup battery becomes low, your device will display warning messages prompting you to replace the backup battery immediately. You can also check the battery status by double-tapping the power status icon if it appears on the taskbar.

Caution:

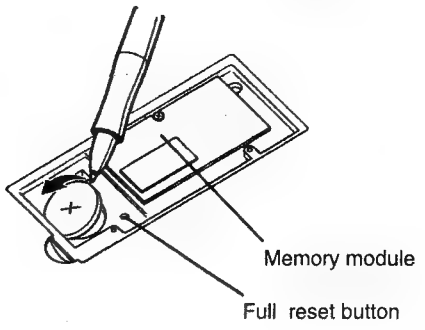
- Before replacing the backup battery, be sure to back up data on the device (for example, to your desktop computer).
- When the low main battery warning message and low backup battery warning message appear at the same time, recharge the main battery first, then reprace the backup battery.

Replacing the backup battery

1. Turn off the device.
2. Using the provided screwdriver, loosen the two backup battery cover screws on the bottom of the device and remove the backup battery cover.



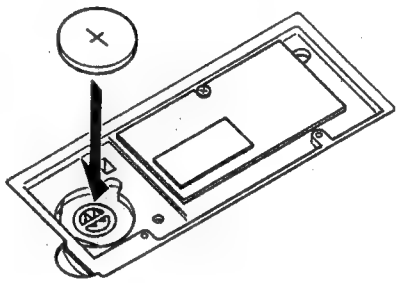
3. Remove the old backup battery with a ballpoint pen.



Caution:

- Do not touch the memory module. Static discharge can destroy it.
- Do not press the **FULL RESET** button; other wise, you will lose all data on the device.

4. Install a new CR2032 lithium memory backup battery.



5. Replace the backup battery cover and fasten it with the two memory module cover screws.
6. After battery replacement, turn on the device and make sure no warning message appears.

Caution:

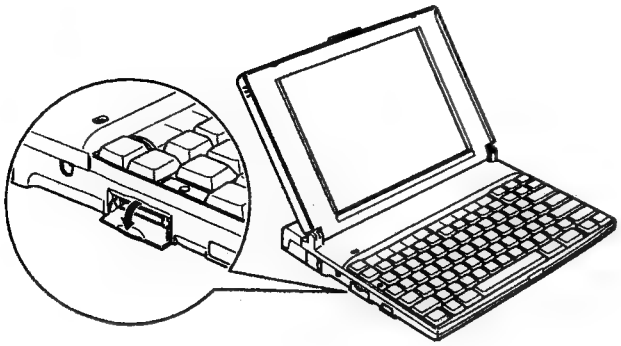
- Keeep batteries out of the reach of children.
- Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
- Backup battery: Replace battery with Panasonic type CR2032 only. Use of another battery may present a risk of fire or explosion. See operation manual for safety instructions.
- Backup battery: Battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire.
- Leaving depleted batteries in the unit may cause battery leakage and damage from corrosion.

3. Connecting the device to your desktop computer

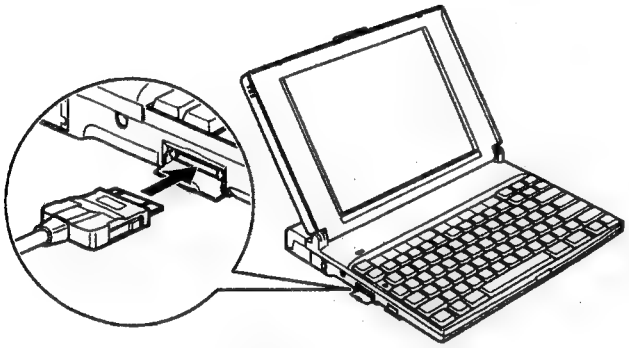
You can connect the device to your desktop computer to backup data, synchronize activities, transfer files, etc. by using Windows CE services.

Connect the device to the desktop computer with the provided serial cable:

1. Turn on the device.
2. Flip open the serial port cover as shown.



3. Insert the 18-pin end of the supplied serial cable into the serial port on the device.



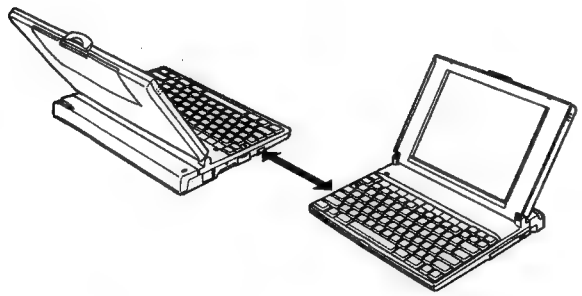
4. Insert the other end of the cable into the serial port on that you plan to specify when you install windows CE services.

4. Using the infrared port for file transfer

You can use the built-in infrared port to transfer files (using Windows Explorer) and cummunicate with other handheld notebook and desktop PCs compliant with the IrDA (115.2 kbps) standards.

Make sure both devices are turned on, then take the following steps:

1. Align the two devices so that their infrared ports are facing each other.



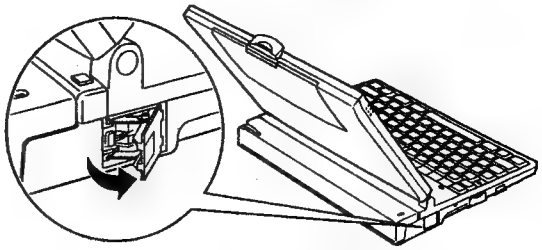
2. From the sending device, tap to select the data of Contacts or the file.
3. On the receiving device, tap **Receive** from the **File** menu.
4. On the sending device, tap **Send** from the **File** menu, or tap **Infrared Recipient** from **Send To** of the **File** menu. Start sending the data.

5. Using the internal fax/modem (May not be available in some countries)

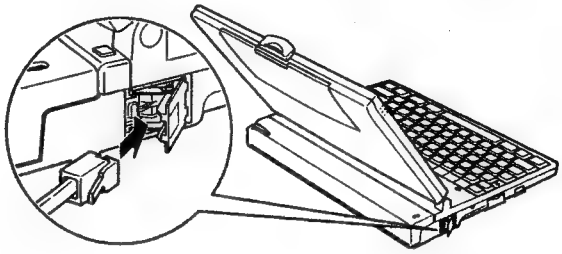
You can use the internal fax/modem to perform fax and data transmission (14.4 kbps for fax and 33.6 kbps for data).

Connect the internal fax/modem to an analog telephone line as follows:

1. Use your finger, gently open the modem port.



2. Insert one end of the supplied modular phone cable into the modem jack.



3. Insert the other end of the modular phone cable into a telephone outlet.

Note:

- Before using the internal fax/modem for communication, check that it is set up in Windows CE.
- The internal modem complies only with North American standards.

Safety Warning on Internal Fax/Modem

- Never install telephone wiring during a lightning storm.
- Never install a modular jack in a wet location unless the jack is specifically designed for wet locations.
- Never touch uninsulated telephone wires or terminals unless the telephone line has been disconnected at the network interface
- Use caution when installing or modifying telephone cables.
- Avois using the modem over a telephone line during an electrical storm. Electronic shock and main unit damage from lightning is possible.
- This Fax/Modem is designed for use with analog telephone systems only. Use with digital telephone systems, often found in offices and hotels, may cause permanent damage. You need to be sure the line you are connecting to is an analog line. Please check with the facilities manager before communicating.
- Do not use the Fax/Modem to report a gas leak in the vicinity of the leak.

6. Using a PC Card

Caution:

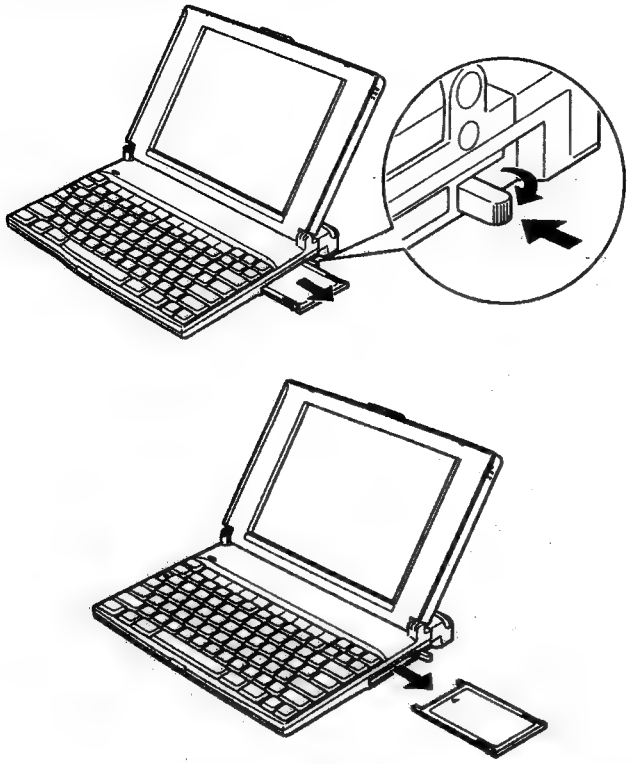
- Not all PC Cards will work with the device. Be sure to use only recommended PC Cards. Using non-recommended PC Cards may cause problems such as damage to the device or the PC Card. Contact your local dealer for more information on recommended PC Cards.
- Some PC Cards such as the optional sharp Digital Cameras Card consume a great deal of power. When using such PC Cards, we recommend you use the AC adaptor whenever possible.
- Depending on the battery level, the display may turn off without display any warning message (such as a low battery warning) when it is used with certain PC Cards that use a great deal of power, such as the Sharp Digital Camera Card.

Removing the Protection Card or a PC Card

A protection Card is inserted into the PC Card slot at the factory for protection.

1. Close all applications accessing or otherwise utilizing, data on the inserted PC Card.

2. Turn off the device.
3. Swing out the PC Card eject button and push it to release the PC Card, then remove the card by hand.



Note:

- Insert the Protection Card in the PC Card slot whenever you do not using a PC Card.
- Do not leave the PC Card slot empty.

Inserting a PC Card

Insert the PC Card into the slot as far as it will go. Make sure the PC Card is facing up. If the card will not go in, check the orientation. Never force the card as it may couse damage to the device or the card itself.

1. Make sure the protection card or a PC Card is not already inserted in the PC Card slot.
2. Insert the PC Card.

3. Swing closed in the PC Card eject button.

7. FLASH ROM SERVICE WRITING/CHECKING PROCEDURES

The procedures are for writing into the FALSH ROM in the PV-5000.

Servicing for the PV-5000 is performed in the following cases:

(1) When the Main PCB unit is replaced.
(2) When the FLASH ROM is replaced.
(3) When the following functions are carried out from the Diag Check.
   1. "No.5 Aging"
   2. "No.33 4Mb FLASH Check"
   3. "No.35 4Mb FLASH Erase"

1) Necessary devices

1. PC (installed Windows CE: MS version CD-ROM)
2. Serial cable
3. PATCH PROGRAM
4. AC Adaptor

2) Operating procedure

<PC SIDE>

1. Start — Program — Microsoft Windows CE services — Mobile device
2. File — Communications — Windows CE services Properties
3. Check the "Enable mobile device connection".
4. Set the "Device Connections via Serial port".

<PV-5000 SIDE>

5. Start — Settings — Control Panel — Communications — PC Connection
6. Set the "Connect using : Serial@115k".
7. Connect the Serial cable between PC and PV-5000.
   In the case of Windows 95/98, the connection is automatically established.
   In the case of Windows NT, "guest" should be input after the login window is displayed.

<PC SIDE>

8. New Mobile Device Detected — Guest — Mobile Devices — Click the Guest
9. The contents of PV-5000 will be displayed.
10. Copy the patch program to PV-5000.

<PV-5000 SIDE>

11. Run the patch program on the PV-5000.
12. Confirm the model type being displayed, then press the ENTER key.

When the patch program is written, PV-5000 automatically restart.

13. Run the patch program once again, and check the patch version is correct.
14. Delete the patch program from PV-5000.

8. ABOUT THE UNIT'S ORIGINAL INITIAL SETTING VALUE.

The unit's original initial setting value (the contrast initial value) is written into the FLASH ROM during the production process.

Normally, this setting value is not erased when service checks are performed.

However, when the Main PCB is exchanged, or the flash ROM on the PCB is exchanged, rewrite the setting value using the following method.

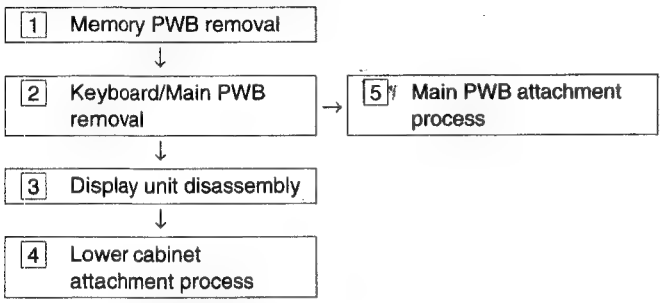
<Contrast Setting>

1. Start the Diag.
2. Select "3. Set Contrast".
3. Adjust the contrast.
4. Use [CTRL]+[W] to write the setting.

CHAPTER 4. DISASSEMBLY AND ASSEMBLY

This chapter mainly describes the disassembly procedure.
For assembly, reverse the disassembly procedures.
If any special care is required for assembly, "Note for assembly" is provided.
Simple and easy replacement procedures of units and parts are omitted.

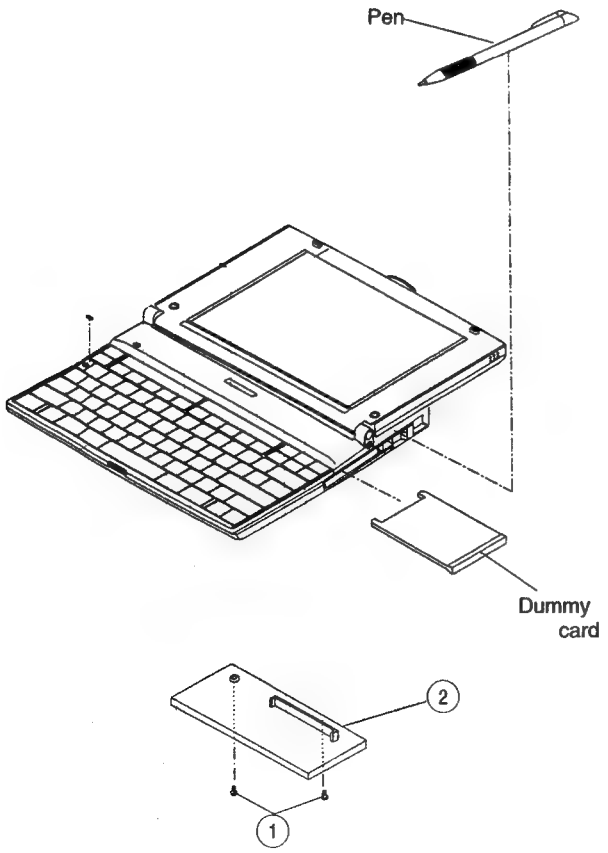
[Flowchart of disassembly]



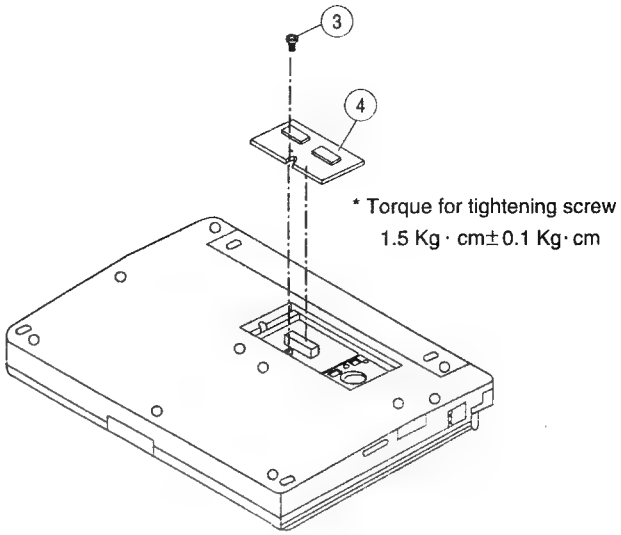
[Note] When the PV-5000 is removed, please attach the "PS starting rubber". The "PS starting rubber" is necessary for power off of PV-5000 Main PWB.

1 Memory PWB removal

1. Remove two screws ①.
2. Remove Battery cover ②.

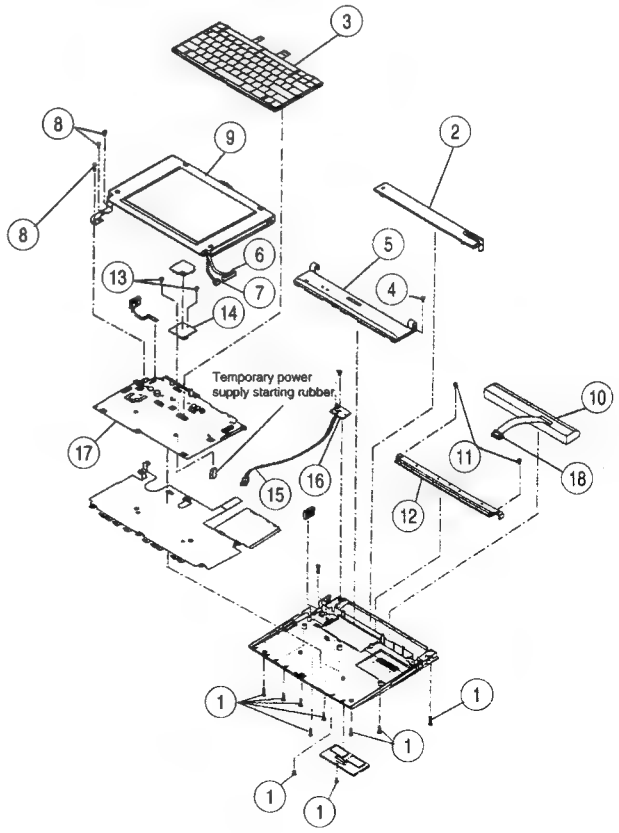


3. Remove one screws ③.
4. Remove memory PWB ④.



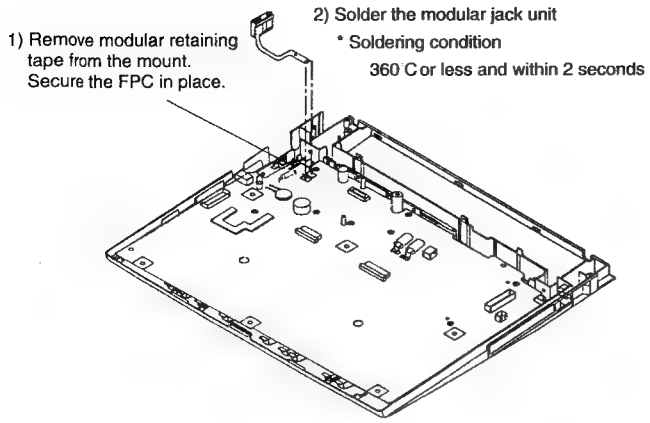
2 Keyboard/Main PWB removal

1. Remove ten screws ①.
2. Remove Battery cabinet unit ②.
3. Remove one screw ④ and remove cabinet A ⑤.
4. Remove keyboard ③ .
5. Remove Main cable ⑥ ⑦ ⑱.
6. Remove three screws ⑧ and remove display unit ⑨.
7. Remove Main battery ⑩.
8. Remove two screws ⑪ and remove cabinet B ⑫.
9. Remove two screws ⑬ and remove BMU PWB ⑭.
10. Remove LED connecter ⑮ and remove battery LED PWB ⑯.
11. Remove Main PWB ⑰.



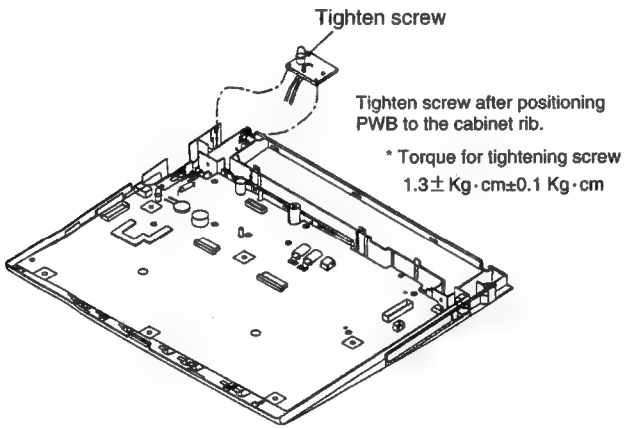
[Note for assembly]

1. Solder modular jack unit to secure

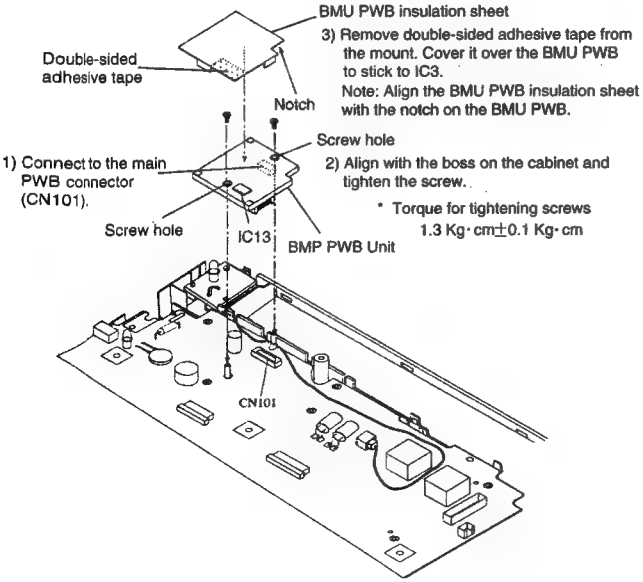


Note: FPC is unstable. Use caution to handle it until it is secured to the cabinet (to prevent the wire from breaking).

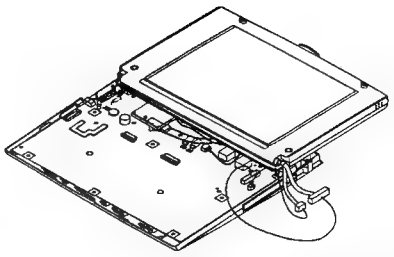
2. Arrange battery LED PWB lead wire



3. Install BMU PWB and attach BMU PWB insulating sheet



4. Connect main cable

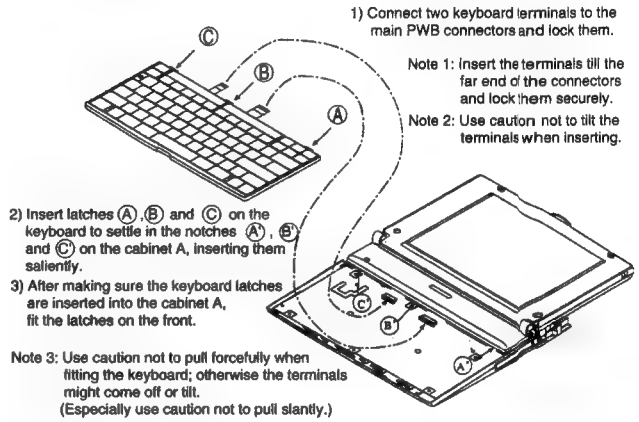


1) Twist the main cable by a complete revolution counterclockwise, along with 4-pin and 40-pin together to connect the connector (to prevent the 4-pin and 40-pin from coming loose).
Connector insertion direction
40-pin connector: White line on the display side
4-pin connector: Connector terminal is shown on the card slot side.

Note 1: Install the connectors securely. Use caution not to bend the terminal when installing the connectors.

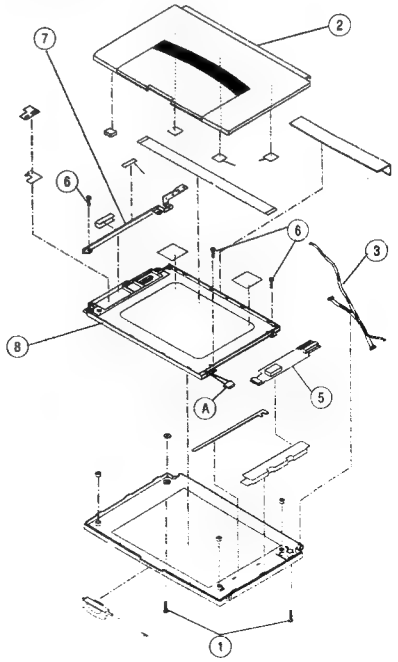
Note 2: Do not pull the cable unnecessarily; otherwise the cable might break.

5. Connect/install/fit key board



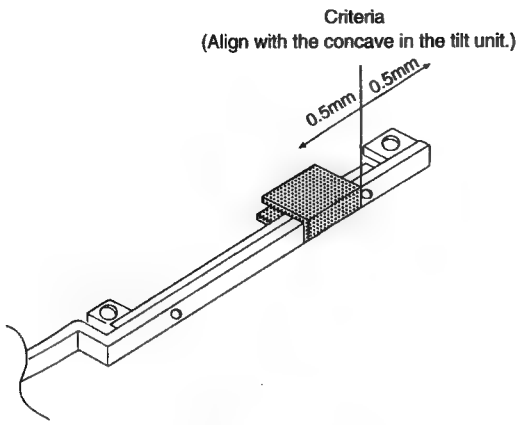
3 Display unit disassembly

1. Remove two screws ① and remove display cover ②.
2. Remove main cable ③ and tablet cable ④.
3. Remove Inverter PWB unit ⑤.
4. Remove three screws ⑥ and remove tilt unit ⑦.
5. Remove LCD+Tablet unit ⑧.



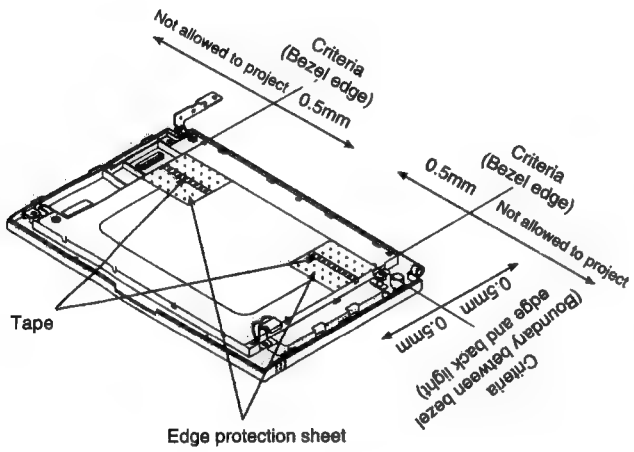
[Note for assembly]

1. Attach edge protection sheet to the tilt unit

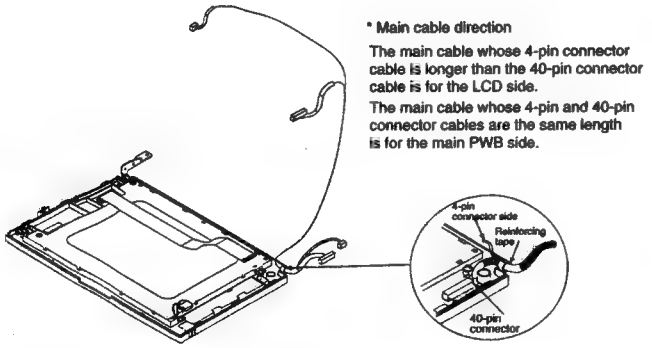


Note 1: Remove grease from the attaching area by IPA before attaching the sheet.

2. Attach edge protection sheet

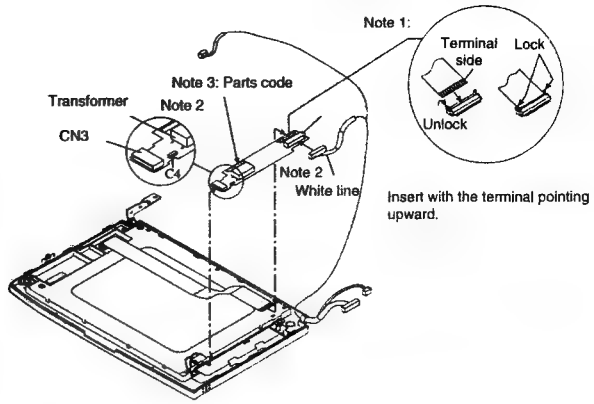


3. Install main cable



1) Install the main cable to the hinge of the display mask, paying attention to the direction.
2) Align the edge of the reinforcing tape with the hinge.

4. Connect LCD cable/main cable/back light unit to inverter PWB



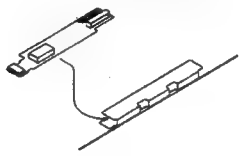
Note 1: Don't lift the lock lever forcefully when unlocking the connector. Use caution not to insert the cable slantly. Lock securely.

Note 2: Hold the connector by hand when connecting CN1/CN3, to prevent C4 and transformer from being stressed.

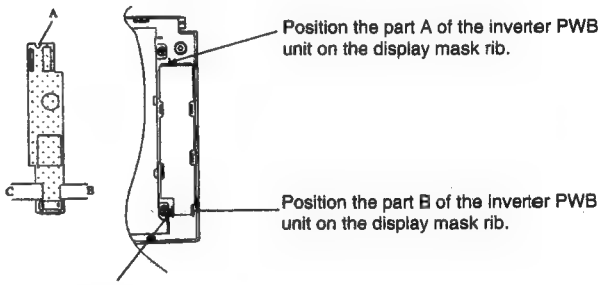
Note 3: Make sure the inverter PWB unit part code is correct: DUNTK1736YCZZ

Note 4: Don't stack up inverter PWB units or twist them tostress; otherwise the transformer wire might break to cause smoke.

5. Install inverter PWB unit inside insulating sheet



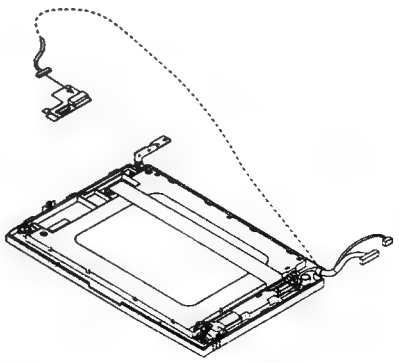
Install the inverter PWB unit inside the insulating sheet.



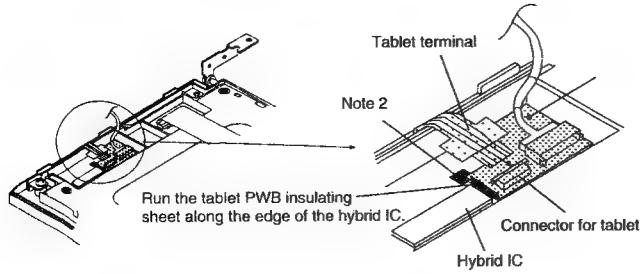
Note 1: Install to prevent the inverter PWB unit from being stressed.

Note 2: Do not pull forcefully; otherwise the connector might be disconnected or unlocked. Use caution not to tilt the connection part.

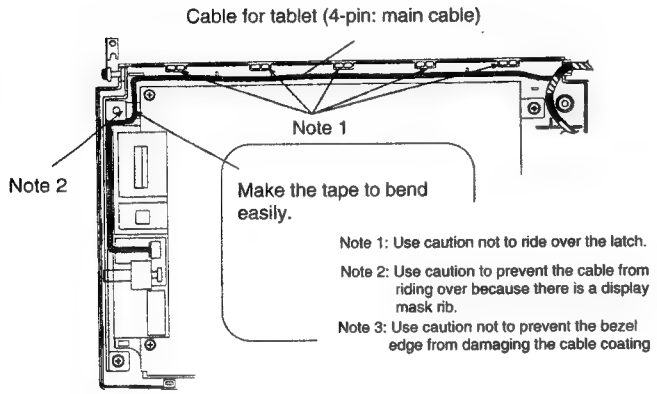
6. Arrange main cable/back light cable wire



7. Install tablet relay PWB/connect tablet terminal

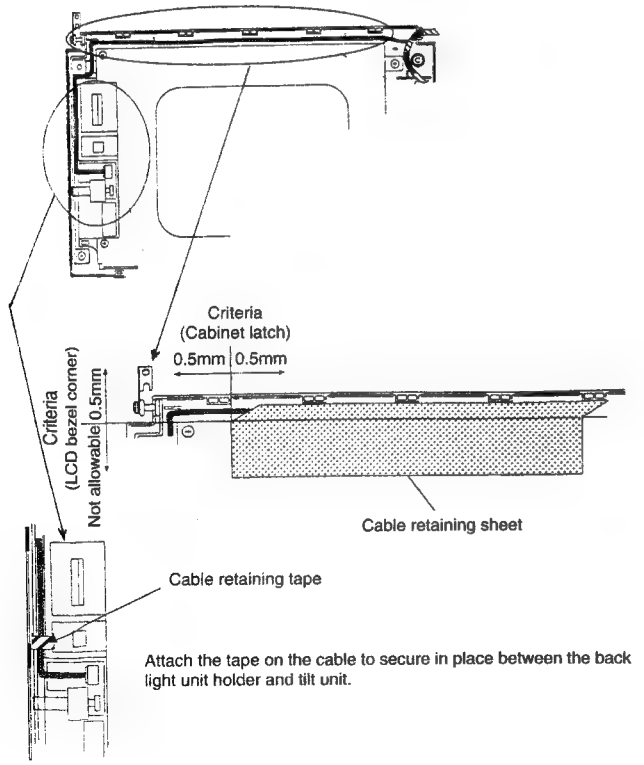


8. Arrange tablet wire (4-pin: main cable)

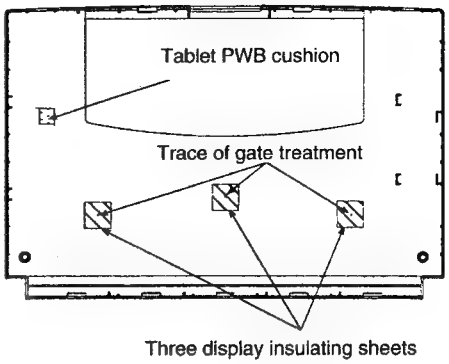


1) Pass between the LCD and cabinet, and the tilt unit and cabinet

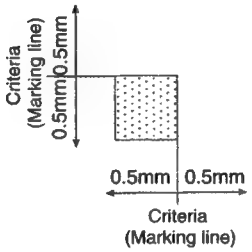
9. Attach cable retaining tape/sheet



10. Attach tablet PWB cushion/display insulation sheet

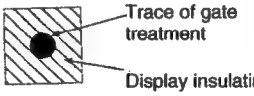


1) Attach tablet PWB cushion



Note 1: Remove grease from the attaching area by IPA before attaching.

2) Attach display insulating sheets



Attach each sheet with the trace of gate treatment positioned at the center of the sheet.

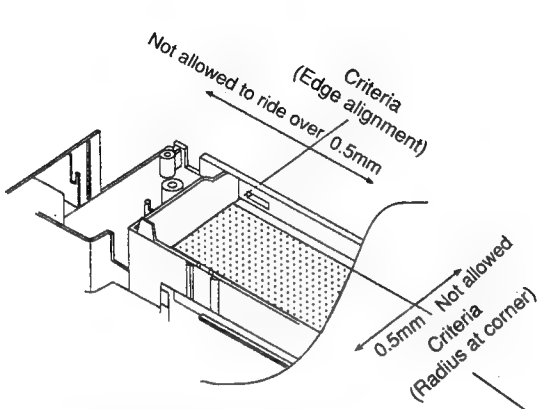
Note 1: Remove grease from the attaching area by IPA before attaching.

Note 2: It is allowable if the trace of gate treatment is located within more than 2mm from the insulating sheet edge.

Note 3: There are eight traces of gate treatment. Use caution not to confuse attached places.

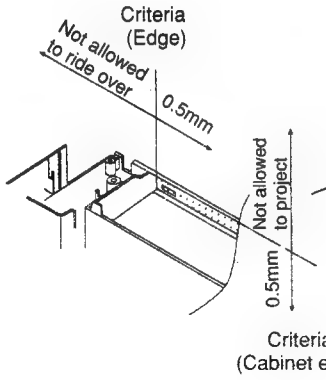
4 Lower cabinet attachment process

1. Attach battery insulating sheet A



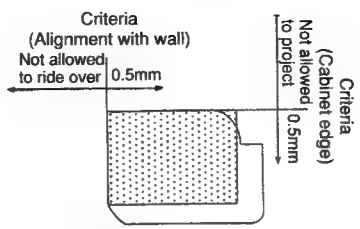
Note 1: Remove grease from the attaching area by IPA before attaching the sheet

2. Attach battery insulating sheet B



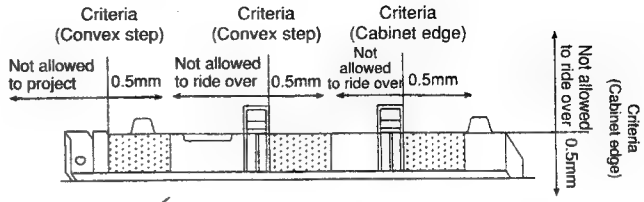
Note 1: Remove grease from the attaching area by IPA before attaching the sheet.

4. Attach battery cushion B



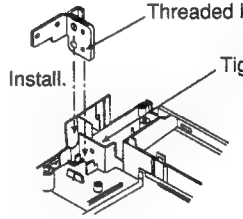
Note 1: Remove grease from the attaching area by IPA before attaching the sheet after

3 .Attach battery cushion A

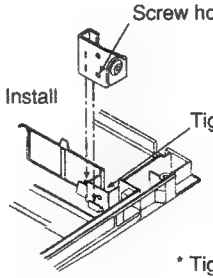


Note 1: Remove grease from the attaching area by IPA before attaching the sheet.

5. Install cabinet securing angle and tighten securing screw (using cradle)



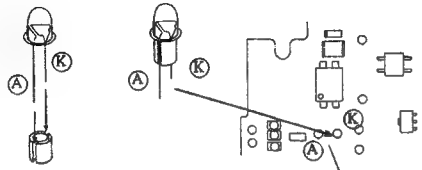
6. Install connection angle and tighten securing screw (using cradle)



* Tightening torque
2.0Kg· cm±0.1 Kg· cm

5 Main PWB attachment process

1.Install and solder LED/LED spacer (using jig)

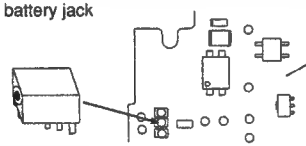


1) Install the LED lead along the LED spacer groove.
2) Insert into the PWB, paying attention to the polarity and solder at the back.
3) After soldering, cut the lead within 1mm from the rear of the PWB. (Soldering condition: 300±5℃, within 3 seconds)
4) After cutting the lead, solder again (to prevent cracking).

Note 1: Make sure the LED is in close contact with the spacer and the spacer with the PWB. Tilt or float is not allowed.

Note 2: Pay attention to the LED polarity (A: anode/K: cathode)

2.Solder battery jack



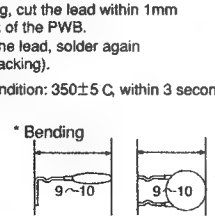
1) Install the positioning pin and terminal into the PWB. Solder at the back of it. (Soldering condition: 350±5℃, within 3 seconds)

Note 1: Make sure the battery jack is in close contact with the PWB. Tilt or float is not allowed.

3.Solder polyswitch

1) Install the polyswitch into the PWB unit hole. Solder at the back of it.
2) After soldering, cut the lead within 1mm from the back of the PWB.
3) After cutting the lead, solder again (to prevent cracking).

(Soldering condition: 350±5℃, within 3 seconds)



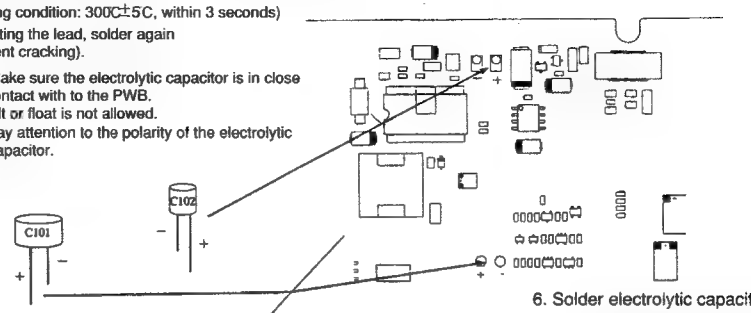
Note 1: Insert the polyswitch lead until completely it reaches the concave.

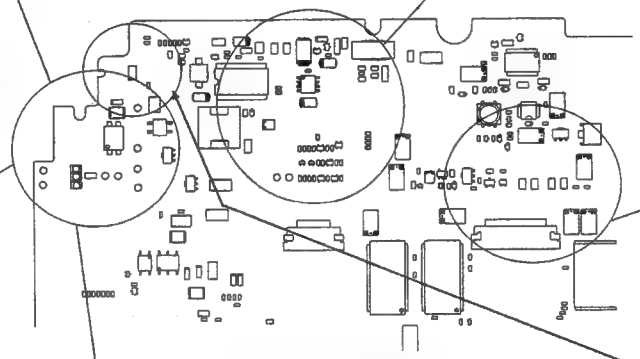
5. Solder electrolytic capacitor (C101:22μF/125V, C102:33 R35V)

1) Insert the electrolytic capacitor into the PWB, paying attention to its polarity and solder it at the back of the PWB.
2) After soldering, cut the lead within 1mm from the back of the PWB. (Soldering condition: 300℃±5℃, within 3 seconds)
3) After cutting the lead, solder again (to prevent cracking).

Note 1: Make sure the electrolytic capacitor is in close contact with to the PWB. Tilt or float is not allowed.

Note 2: Pay attention to the polarity of the electrolytic capacitor.

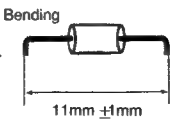




4. Solder surge suppresser

1) Install the surge suppresser into the PWB unit hole. Solder it at the back of it.
2) After soldering, cut the lead within 1mm from the back of the PWB.
3) A fter cutting the lead, solder again (to prevent cracking). (Soldering condition: 350±5℃, within 3 seconds)

Note 1: After installing the lead on the ⓐ side when securing the PWB temporally, bend to inside. If bent to outside, it touches chassis when cutting the lead incompletely.

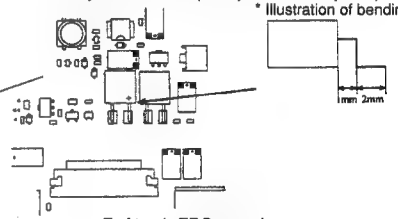


6. Solder electrolytic capacitor (C32, C33:33μ/35V)

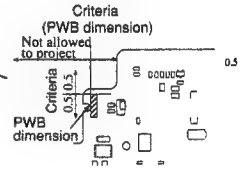
1) Form the electrolytic capacitor according to the illustration below, paying attention to the polarity and solder. (Soldering condition: 350℃±5℃, within 3 seconds)

Note 1: Make sure the electrolytic capacitor is in close contact with the PWB. Tilt or float is not allowed.

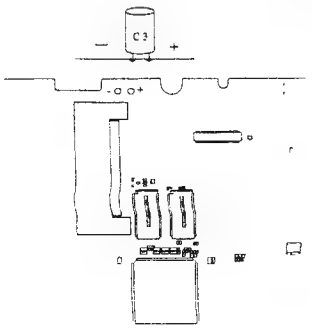
Note 2: Pay attention to the polarity of the electrolytic capacitor.



7. Attach FPC securing tape



Note 1: Use caution to prevent the entrance of foreign material



1. Soldering electrolytic capacitor (C3:33 μ /35V)

1) Insert the electrolytic capacitor into the PWB, paying attention to the polarity, and solder at the back of the PWB.
2) After soldering, cut the lead within 1mm or less distance from the back of PWB. (Soldering condition: 300℃±5℃, within 3 seconds)
3) After cutting the lead, solder again (to prevent cracks).

Note 1: Make sure the electrolytic capacitor is in close contact with the PWB. Tilt or float is not allowed.

Note 2: Pay attention to the polarity of the electrolytic capacitor.

CHAPTER 5. DIAGNOSTICS AND CHECK ITEMS

ROM CHECK, 4Mb FLASH CHECK

No	Operating procedure	Display	Check item
1	Attach the AC adaptor. Enter the Normal diag mode with "2" +"W" + RESET.	Diag menu	Check the display of "Exec Mode : ROM".
2	Touch "18. ROM CHECK (FULL)".	=== ROM CHECK full === << CHECK:ROM block0 [ ] [ ] ...OK >> << CHECK:ROM block1 [ ] [ ] ...OK >> << CHECK:ROM block2 [ ] [ ] ...OK >>	Check the display of "OK".
3	Press the POWER key.	Diag menu	
4	Touch "33. 4Mb FLASH CHECK".	=== 4Mb Flash Check === [CHECK 1] ...OK [CHECK 2] ...OK	Check the display of "OK".
5	Press the POWER key.	Diag menu	
6	Press the POWER key. Remove the AC adaptor.	Display OFF	

Note: When "33. 4Mb FLASH CHECK" are executed on the diag, a patch of data will be cleared.

LCD CHECK

No	Operating procedure	Display	Check item
1	Attach the AC adapter. Enter the Normal diag mode with "2" + "W" + RESET.	Diag menu	
2	Touch "2. LCD CHECK".	Color bar	Check the display for no defects.
3	Press the ENTER key.	Red	Check the display for no defects and blurs.
4	Press the ENTER key.	Green	Check the display for no defects and blurs.
5	Press the ENTER key.	Blue	Check the display for no defects and blurs.
6	Press the ENTER key.	White	Check the display for no defects and blurs.
7	Press the ENTER key.	Black	Check the display for no defects and blurs.
8	Press the ENTER key.	Gray 16-gradation display	Check the display for no defects and blurs.
9	Press the ENTER key.	Red 16-gradation display	Check the display for no defects and blurs.
10	Press the ENTER key.	Green 16-gradation display	Check the display for no defects and blurs.
11	Press the ENTER key.	Blue 16-gradation display	Check the display for no defects and blurs.
12	Press the ENTER key.	Plover (2 × 2)	Check the display for no defects and blurs.
13	Press the ENTER key.	Plover rotation (2 × 2)	Check the display for no defects and blurs.
14	Press the ENTER key.	Vertical black	Check the display for no defects
15	Press the ENTER key.	Horizontal black	Check the display for no defects
16	Press the ENTER key.	Plover with fluctuated density	Check that the display density changes smoothly.
17	Press the ENTER key.	<VRAM CHECK> oblique color line LCD VRAM Check OK (except Half Frame Buffer)	Check the display for no error.
18	Press the POWER key.	Diag menu	
19	Press the POWER key. Remove the AC adaptor.	Display OFF	

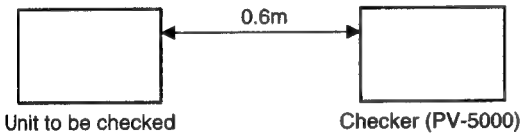
KEYBOAD CHECK

No	Operating procedure	Display	Check item
1	Attach the AC adapter. Enter the Normal diag mode with "2" + "W" + RESET.	Diag menu	
2	Touch "4. KEYBOAD CHECK".		
3	Press the key in displayed screen.		Check the input of all keys.
4	Press the POWER key.	Diag menu	
5	Press the POWER key. Remove the AC adaptor.	Display OFF	

IR CHECK

No	Operating procedure	Display	Check item
1	Attach the AC adapter. Enter the Normal diag mode with "2" + "W" + RESET.	Diag menu	
2	Touch "7.IR CHECK". (Checker) Touch "31. IR CHECKER".	=== IR CHECK (Slave) === Push [Y] key to retry 1 checking...OK	Check the display of "OK".
3	Press the POWER key.	Diag menu	
4	Press the POWER key. Remove the AC adaptor.	Display OFF	

Note: The figure below shows the arrangement for IR check.



PCMCIA CONNECTOR CHECK

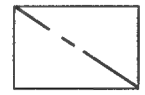
No	Operating procedure	Display	Check item
1	Attach the AC adapter. Enter the Normal diag mode with "2" + "W" + RESET.	Diag menu	
2	Enter the product diag mode with "Ctrl" + "Alt" + "A2".		
3	Install a 1MB S-RAM card.		
4	Touch "10.RAM CARD CHECK WRITE".	= PCMCIA RAM CHECK (full) Write = 1Mbytes PCMCIA RAM CARD Now writing data.....OK	Check the display of "OK".
5	Press the POWER key.	Diag menu	
6	Touch "11. RAM CARD CHECK READ".	= PCMCIA RAM CHECK (full) Read = 1Mbytes PCMCIA RAM CARD Now reading & checking data ..0000....OK	Check the display of "OK".
7	Press the POWER key. Remove the AC adaptor.	Display OFF	

Note: The write protect SW of the card must be released. (Not protected.)

SPEAKER CHECK

No	Operating procedure	Display	Check item
1	Attach the AC adapter. Enter the Normal diag mode with "2" + "W" + RESET.	Diag menu	
2	Touch "10. SPEAKER TEST".	[1] OFF [2] 300Hz [3] 1kHz [4] 3kHz	
3	Press the [4] key.		Standard: The reproduced sound must be clear.
4	Press the [1] key.		

TABLET CHECK

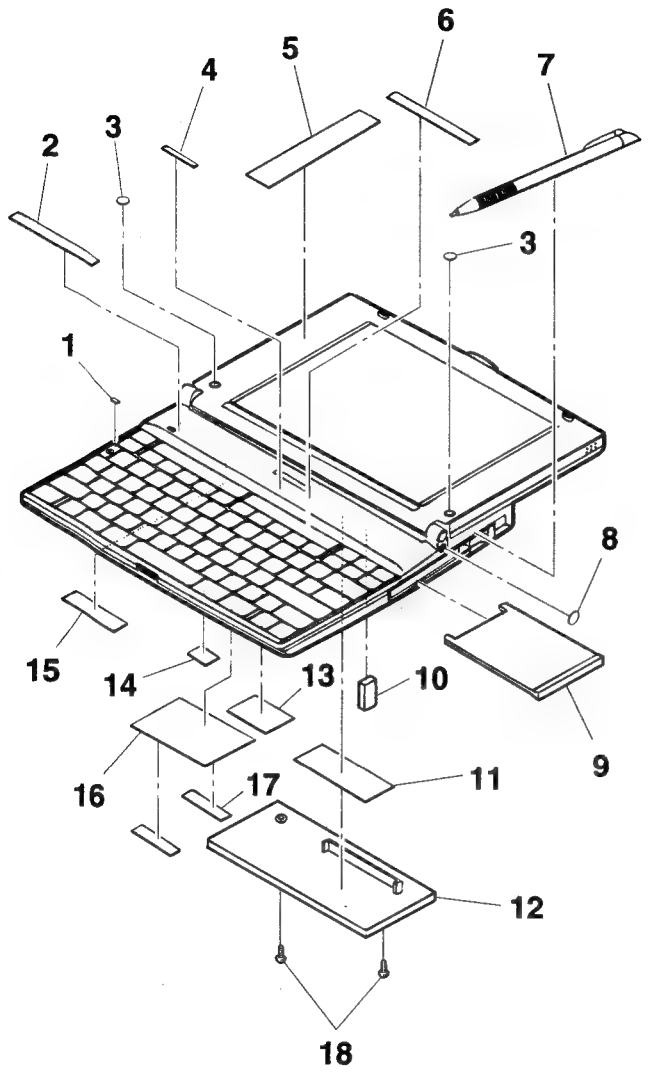
No	Operating procedure	Display	Check item
1	Press the POWER key.	OS screen	
2	Enter the tablet adjust screen with "Ctrl" + "Alt" + "=" in the SETUP WIZARD INTRODUCTION SCREEN.		
3	Touch [+]	Adjust by [+] mark.	Check the input by tablet. Input the center of [+] mark.
4	Press the ENTER key.		
5	Start the "Image Editor". "Win" key - Tablet Programs - SHARP Applications - Image Editor	Image Editor Application	
6	Draw two lines ; left upper right lower and left lower right upper.		○  Draw a straight line without deflection. ×  If the line deflects, put a slightly stronger pressure on the pen and draw a line again. ×  If the line is cut out, move the pen more slowly and draw a line again. ×  If there is a shift between the line and the pen, perform the tablet check from the beginning to check again.
7	Press the POWER key.	Display OFF	

PV-50
PV-50A
PV-
Exteriors

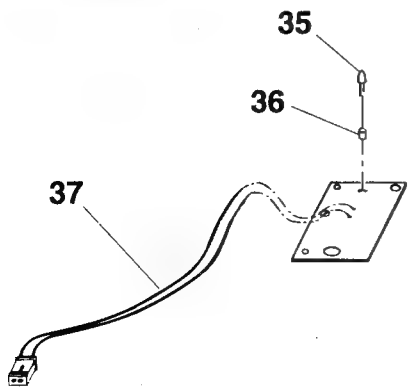
1

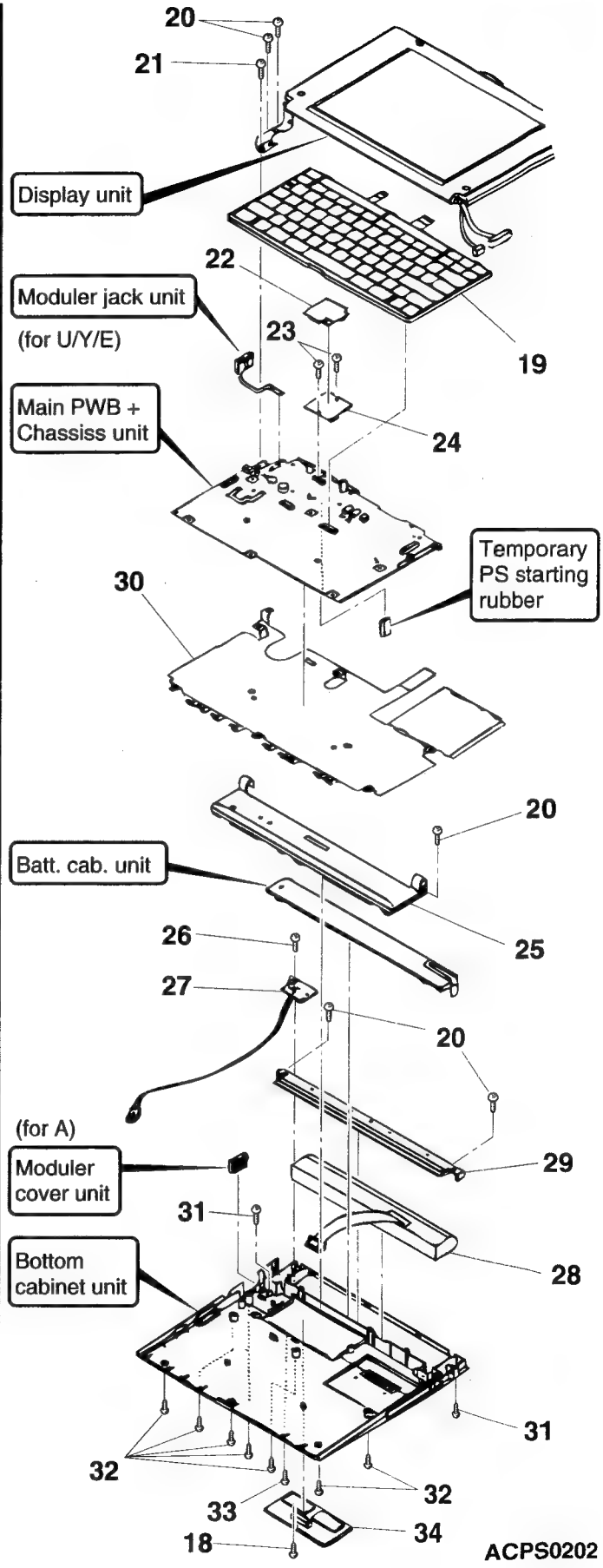
	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
2	TLABZ1214YCZZ	AD	N	D	Reset label	
3	TLABZ1211YCZZ	AE	N	D	Function label A	
4	PSHEZ1052YCZZ	AC	N	C	Screw blind aheet L	
5	TLABZ1215YCZZ	AC	N	D	Mobilon pro label	[U.S.A,Canada]
6	TLABZ1216YCZZ	AF	N	D	Sales label	
7	TLABZ1212YCZZ	AE	N	D	Function label B	
8	CPENP1004PCN8	AG		C	Pen	
9	PSHEZ1051YCZZ	AB	N	C	Screw blind aheet H	
10	GiTAZ1124LCZB	AF	N	C	Dummy card	
11	PGUMM1014YCZZ	AC	N	C	PS starting rubber	
12	TLABZ1220YCZZ	AD	N	D	Full reset caution label	
13	GFTAB1043YCZZ	AK	N	D	Battery cover	
14	TLABS1193YCZZ	AD		D	EMI label	[Canada]
15	TLABZ1218YCZZ		N	D	IC label	[Canada]
16	TLABZ1101YCZZ	AC		D	UL battery label	
	TLABM1210YCZZ	AE	N	D	Name plate label	[PV-5000]
	TLABM1227YCZZ	AF	N	D	Name plate label	[PV-5000A]
17	TLABS1213YCZZ	AC	N	D	FCC No.label	[PV-5000]
18	LX-BZ1019YCZZ	AB		C	Screw (M3.8)	
19	DUNT-1745YCZZ	BH	N	E	Key unit	
20	LX-BZ1034LCZZ	AC		C	Screw (M2×L3.5)	
21	LX-BZ1035LCZZ	AC		C	Screw (M2.6×L6)	
22	PZETL1043YCZZ	AF	N	C	BMU PWB insulation sheet	
23	LX-BZ1193CCZZ	AA		C	Screw (M1.7)	
24	DUNTK1750YCZZ	BT	N	E	BMU PWB unit	
25	CCABA1144LC03	AV	N	D	Top cabinet ass'y A	(include No.101)
26	LX-BZ1279CCZZ	AA		C	Screw	
27	DUNTK1749YCZZ		N	E	LED sub PWB unit	(include No.35~37)
28	UBATi1009YCZZ	BK	N	B	Li-battery	
29	CCABA1150LC03	AS	N	D	Top cabinet ass'y B	
30	PSLDC1092LCZB	AN	N	C	Shield plate(bottom)	
31	LX-BZ1023YCZZ	AB	N	C	Screw	
32	LX-BZ1033LCZZ	AA		C	Screw (M2.6×L7)	
33	LX-BZ1039LCZZ	AC		C	Screw (M2.6×L4)	
34	DUNTK1741YCZZ		N	E	Memeory PWB unit	
35	VHPGL3HS43/-1	AB		B	LED (Orange) (GL3HS43)	
36	PSPAZ1108LCZZ	AD		C	LED spacer	
37	QCNW-1024YCZZ	AD	N	C	LED cable	
101	PFiLW1075LCZA	AE	N	D	LED filter	(for Top cabnet ass'y A)

1 Exteriors



Battery LED PWB unit





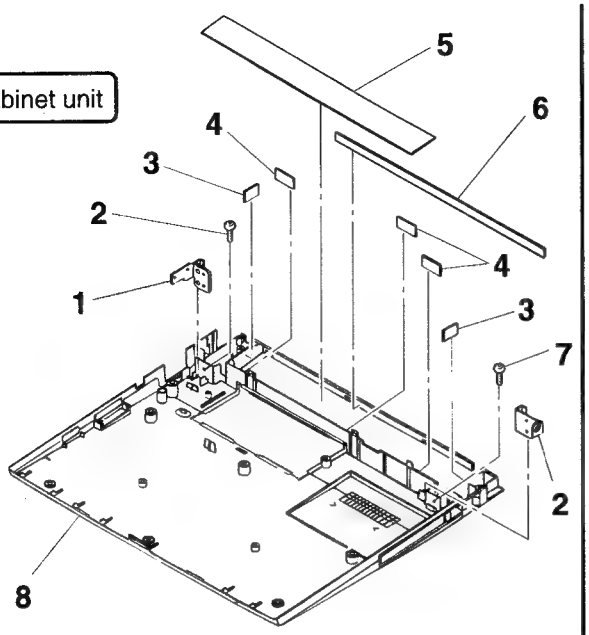
PV-5000
PV-5000A

2 Bottom cabinet etc.

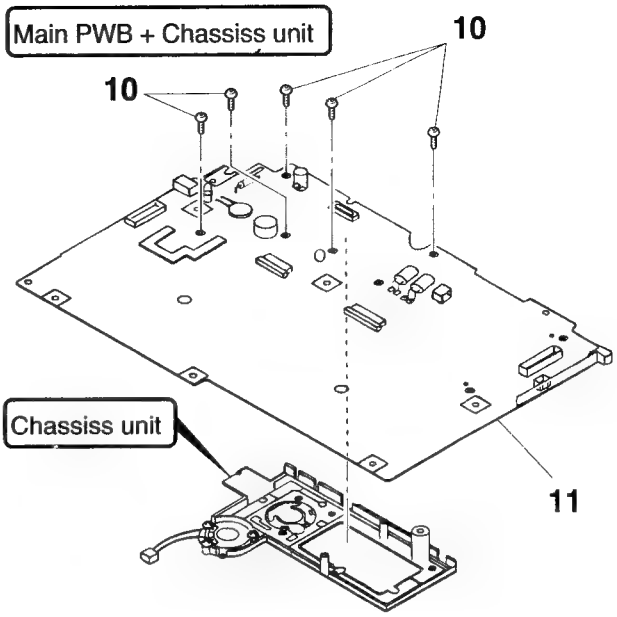
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LANGT1296LCZA	AH	N	C	Cabinet fixing angle L
2	LANGT1297LCZZ	AF		C	Fixing angle R
3	PCUSS1053YCZZ	AC	N	C	BT fixing cushion B
4	PCUSS1052YCZZ	AC	N	C	BT fixing cushion A
5	PZETL1040YCZZ	AD	N	C	Battery insulation sheet A
6	PZETL1041YCZZ	AC	N	C	Battery insulation sheet B
7	LX-BZ1034LCZZ	AC		C	Screw (M2×L3.5)
8	CCABB1074YC01	BC	N	D	Bottom cabinet ass'y (include No.101,102)
10	LX-BZ1002PCZZ	AA		C	Screw (M1.7 L=3.4)
11	DUNTK1784YCZZ		N	E	Main PWB unit (include No.12~14,16~18,20,21)[U.S.A]
	DUNTK1738YCZZ		N	E	Main PWB unit (include No.12~14,16~18,20,21)[Canada,Hong Kong]
	DUNTK1752YCZZ		N	E	Main PWB unit (include No.12~14,16~18,20,21)[PV-5000A]
12	PZETL1046YCZZ	AC	N	C	Main insulation sheet
13	QJAKC1010YCZZ	AF	N	C	PS jack
14	PSPAZ1108LCZZ	AD		C	LED spacer
15	PTPEH1067YCZZ	AB	N	D	FPC fixing tape [PV-5000]
16	XBBSD20P06000	AA		C	Screw (2×6)
17	PGiDM1032LCZZ	AR		C	PC ejector
18	PSHEZ1400LCZA	AE		C	PC insulation sheet
19	PZETL1044YCZZ	AC	N	C	Insulation sheet (18pin)
20	QTANZ1598CCZZ	AB		C	Battery terminal(back up) c
21	QTANZ1604CCZZ	AC		C	Battery terminal(back up) d
22	LX-BZ1010YCZZ	AB		C	Screw
23	VSP0022P-03WG	AQ		B	Speaker
24	LCHSM1011YCZZ	AG	N	D	Chassiss
25	QJAKT1008YC01	AL	N	C	Moduler jack [PV-5000]
26	PCUSS1058YCZZ	AC	N	C	Modem holding cushion
27	PZETL1047YCZZ	AC	N	C	Modem insulation sheet [PV-5000]
28	QPWBM1039YCA1	AG		C	Moduler FPC [PV-5000]
29	GFTAA1031YCZ1	AE	N	D	Moduler cover [PV-5000A]
30	LX-BZ1279CCZZ	AA		C	Screw
31	LHLDZ1032YCZZ	AH	N	C	Pen holder
32	CCABA1072YC01	AW	N	D	Battery cabinet ass'y (include No.103)
101	GFTAZ1085LCZA	AE	N	D	Oustside connection cover
102	PFiLW1074LCZZ	AE		D	IR filter
103	PFiLW1075LCZA	AE	N	D	LED filter (for batt.cab unit)

2 Bottom cabinet etc.

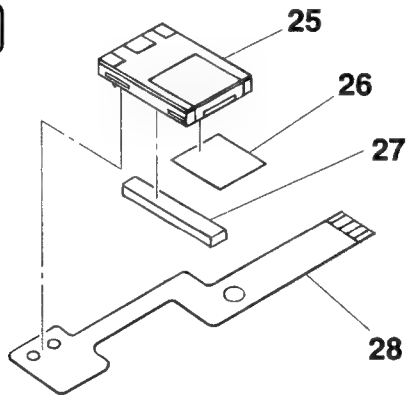
Bottom cabinet unit



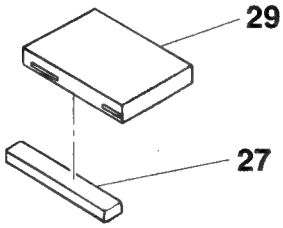
Main PWB + Chassiss unit



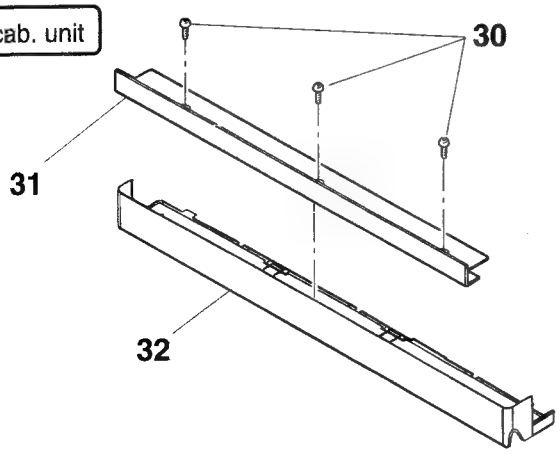
Moduler jack unit
(for U/Y/E)



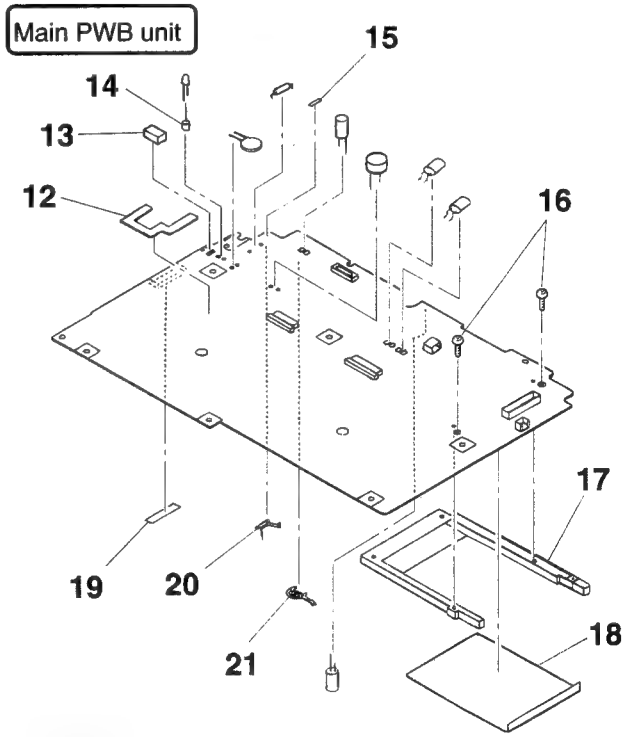
Moduler cover unit
(for A)



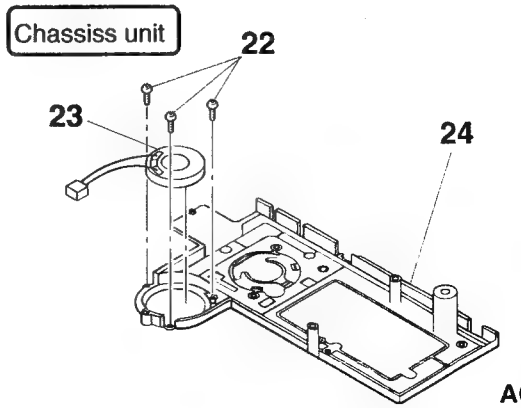
Batt. cab. unit



Main PWB unit

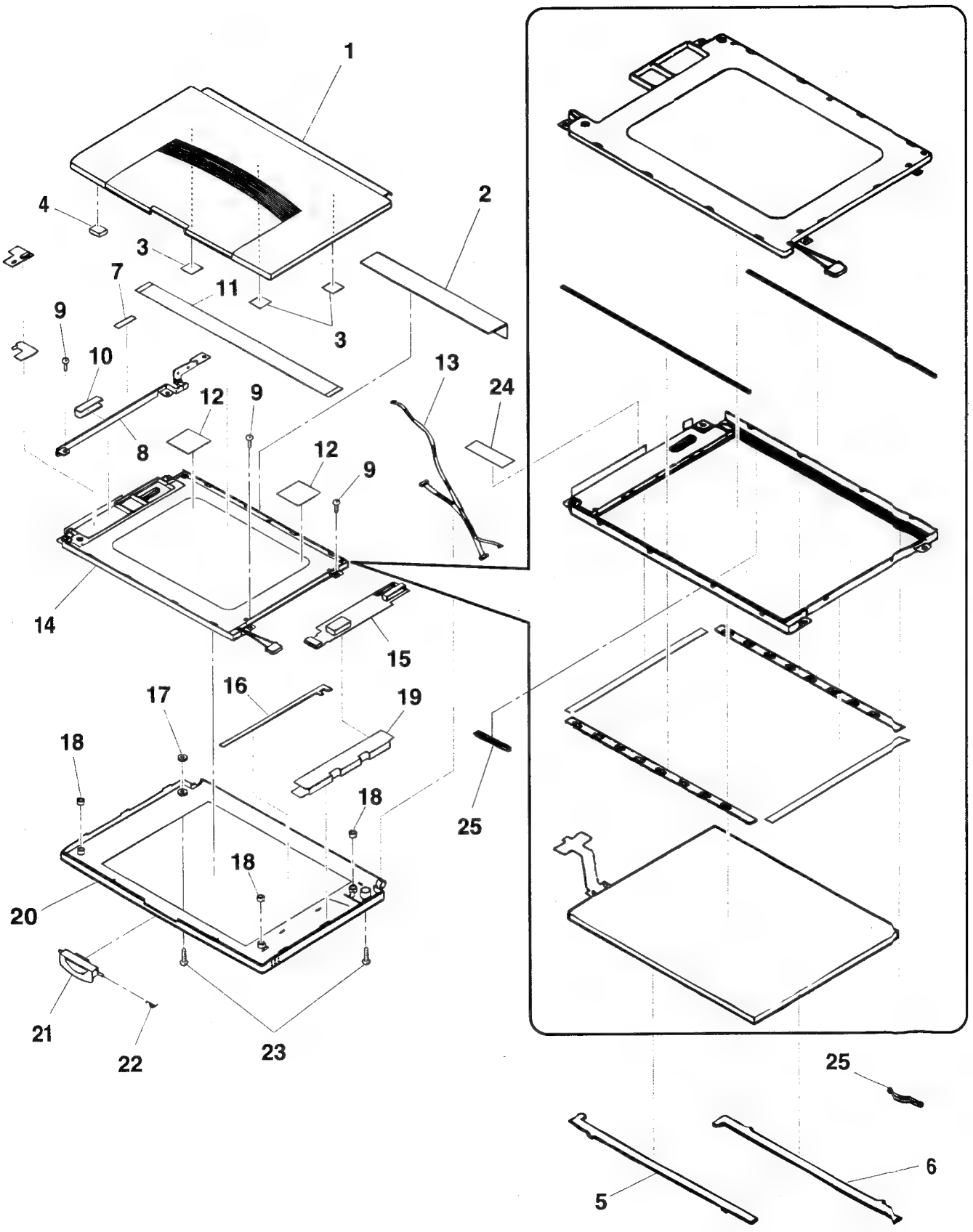


Chassiss unit



ACPS0203

3 Display unit



AC PS0204

3 Display unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	CCABC1071YC01	BD	N	D	Display cover ass'y
2	PSHEZ1057YCZZ	AF	N	C	Wire holding sheet
3	PZETL1048YCZZ		N	C	Display insulation sheet
4	PCUSS1056YCZZ	AB	N	C	Tablet PWB cushion
5	PSPAP1055YCZZ	AG	N	C	Cabinet spacer A
6	PSPAP1056YCZZ	AD	N	C	Cabinet spacer B
7	PTPEH1064YCZZ	AB		D	Tape
8	MHNG-1006YCZZ	AV	N	C	Tilt unit
9	LX-BZ1035LCZZ	AC		C	Screw (M2.6xL6)
10	PSHEZ1056YCZZ	AF	N	C	Edge sheet
11	QCNW-1348LCZZ	AN		C	LCD cable
12	PSHEZ1058YCZZ	AD	N	C	Edge protection sheet
13	QCNW-1023YCZZ	BA	N	C	Main cable
14	DUNT-1744YCZZ		N	E	LCD + Tablet unit (include No.102)
15	DUNTK1736YCZZ	BE	N	E	Invertor PWB unit
16	PSPAP1057YCZZ	AC	N	C	Cabinet spacer C
17	PCAP-1004YCZZ	AC	N	D	Cap B
18	PCAP-1003YCZZ	AC	N	D	Cap A
19	PSHEZ1395LCZA	AF		C	Invertor insulation sheet
20	CCABC1146LC03	BB	N	D	Display mask ass'y (include No.101)
21	GiTAZ1119LCZA	AK		D	Buckle
22	MSPRP1100LCZZ	AC		C	Buckle spring
23	LX-BZ1022YCZZ	AC	N	C	Screw
24	PZETL1023YCZZ	AA		C	Insulation sheet
25	PCUSS1055YCZZ	AC	N	C	Tablet cushion
101	TLABP1209YCZZ	AD	N	D	Function label
102	DUNTB1748YCZZ	BP	N	E	Back light

4 Packing material & Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	TiNSE1181YCZZ	AM	N	D	Instruction book(English)
2	SPAK-1285PCZZ	AA		D	Vinyl bag (for Screw)
3	SPAKA1416YCZZ	AK	N	D	Packing add R
4	SPAKA1417YCZZ	AK	N	D	Packing add L
5	SPAKA1418YCZZ	AF	N	D	Accessory case [U.S.A,Cnada]
	SPAKA1427YCZZ	AF	N	D	Accessory case [Hong Kong,PV-5000A]
6	SPAKA1419YCZZ	AD	N	D	Accessory add
7	SPAKA399ACCZZ	AB		D	Vinyl bag (for SET)
8	SPAKC1420YCZZ	AL	N	D	Packing case
9	SSAKA0006UCZZ	AA		D	Vinyl bag (50x60mm) (for back up battery)
10	SSAKA5004CCZZ	AA		D	Vinyl bag (100x300mm) (for AC cord,Serial/Moduler cable)
11	CDSKA1024YC01	AN	N	D	CD-ROM (SHARP ver.)
⚠ 12	DUNTK4613ACZA	BM		E	AC adaptor
⚠	QACCD1311QCZZ	AN		B	AC cord (10A Bush2M) [U.S.A,Canada]
⚠ 13	QACCB3321QCZZ	BA		B	AC cord (13A BUSH2M) [Hong kong,PV-500A(U.Kingdom,Germany)]
⚠	QACCL3321QCZZ	AR		B	AC cord (7.5A BUSH2M) [PV-5000A(Australia)]
14	QCNW-1015YCZZ	BA		C	Serial cable
15	QCNW-1016YCZZ	AH		C	Moduler cable [except PV-5000A]
16	TCADU1251YCZZ	AE	N	D	User card [U.S.A]
	TCADU1115YCZZ	AG		D	User card [Canada]
	TCADU1256YCZZ	AE	N	D	User card [PV-5000A(Australia)]
17	TCADZ1145YCZZ	AB		D	ELUA caution card
18	TCADZ1250YCZZ	AD	N	D	Set up guide
19	TCADZ1254YCZZ	AC	N	D	BSQUA quick guide
20	TCADZ1255YCZZ	AG	N	D	Free coupon [U.S.A]
21	TLABZ1221YCZZ	AH	N	D	Packing case label [U.S.A]
	TLABZ1222YCZZ	AH	N	D	Packing case label [Canada]
	TLABZ1223YCZZ	AG	N	D	Packing case label [Hong Kong]
	TLABZ1225YCZZ	AG	N	D	Packing case label [PV-5000A]
22	UKOGD1027YCZZ	AH	N	S	Driver c
24	TGANE1114CCN1	AB		D	Warranty card [PV-5000A(Australia)]
	TGANE1003QCZ1	AF		D	Warranty card(EU) [PV-5000A(U.Kingdom,Germany)]
	TGANE1034YC01	AP	N	D	Warranty card [PV-5000A(U.Kingdom)]

PV-5000
PV-5000A

5 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	PGiDM1032LCZZ	AR		C	PC ejector
2	PSHEZ1400LCZA	AE		C	PC insulation sheet
3	PSPAZ1108LCZZ	AD		C	LED spacer
4	PZETL1046YCZZ		N	C	Main insulation sheet
5	QCNCM1047LC0B	AD		C	Connector (2pin) [CN303]
	QCNCM1047LC0B	AD		C	Connector (2pin) [CN103]
6	QCNCM1050YC80	AN		C	Connector (80pin) [CN501]
7	QCNCM1056YC04-	AD	N	C	Connector (4pin) [CN302]
8	QCNCM1153LC6H	AP		C	Connector (PCMCIA)(60pin) [CN701]
9	QCNCM1154LC4J-	AN	N	C	Connector (LCD)(40pin) [CN601]
10	QCNCW1039YCZZ	AN		C	Connector (RS232C) [CN801]
11	QCNCW1057YC18-	AF	N	C	Connector (KEY)(18pin) [CN503]
12	QCNCW1058YC10-	AF	N	C	Connector (KEY)(10pin) [CN502]
13	QCNCW1060YC15-	AH	N	C	Connector (15pin) [CN101]
⚠ 14	QFS-L1019YCZZ	AG		A	Fuse (MMCT2.5A) [F103,102A]
⚠ 15	QFS-L1024YCZZ-	AF	N	A	Fuse (125mA(3216)) [F8]
16	QJAKC1010YCZZ	AF	N	C	PS jack
17	QSW-P1012PCZZ	AE		B	Push switch [SW101]
18	QSW-P1039YCZZ-	AE	N	B	Initialize switch [SW201]
19	QTANZ1598CCZZ	AB		C	Battery terminal(back up) c
20	QTANZ1604CCZZ	AC		C	Battery terminal(back up) d
21	RC-EZ2261RC1E	AL		C	Capacitor (25WV 22μF)(25SL22M)
22	RC-EZ3361RC0K-	AK	N	C	Capacitor (8WV 33μF) [C16,11,13,908,9]
23	RC-EZ3362RC1V	AD		C	Capacitor (35WV 33μF)
24	RC-EZ4762RC0J	AK		C	Capacitor (6.3WV 47μF) [C713,712,407,14,235,406,31,15]
	RC-EZ4762RC0J	AK		C	Capacitor (6.3WV 47μF) [C503,17,611,217,218,216,219,612]
25	RC-KZ1045RC2E	AE		C	Capacitor (25WV 0.1μF) (except PV-500A)[C329]
26	RC-KZ1051RC1H	AC		C	Capacitor (50WV 1μF) [C215]
	RC-KZ1051RC1H	AC		C	Capacitor (50WV 1μF) [C903,106,904,901,105,902]
27	RC-KZ1053RC1E-	AC	N	C	Capacitor (25WV 1μF) [C317,804,335,805,802,801,803]
	RC-KZ1053RC1E-	AC	N	C	Capacitor (25WV 1μF) [C25,24,35,34,36,4,37]
28	RC-KZ1061RC1E-	AK	N	C	Capacitor (25WV 10μF) (except PV-500A)[C333]
29	RC-KZ2241RC1H-	AB	N	C	Capacitor (50WV 0.22μF) [C816]
	RC-KZ2241RC1H-	AB	N	C	Capacitor (50WV 0.22μF) [C110,116]
30	RC-KZ4742RC1H-	AF	N	C	Capacitor (50WV 0.47μF) [C115]
	RC-KZ4742RC1H-	AF	N	C	Capacitor (50WV 0.47μF) [C114]
31	RC-KZ4752RC1A	AE		C	Capacitor (10WV 4.7μF) [C324,319,318,325]
	RC-KZ4752RC1A	AE		C	Capacitor (10WV 4.7μF) [C327,12]
32	RC-SZ1051RC1H-	AG	N	C	Capacitor (50WV 1.0μF) (except PV-500A)[C330]
33	RC-SZ1061RC1A	AF		C	Capacitor (10WV 10μF) [C817]
	RC-SZ1061RC1A	AF		C	Capacitor (10WV 10μF) [C326,304,5,111,609,613,606,213,03,30,328]
34	RC-SZ1061RC1C	AF		C	Capacitor (16WV 10μF) [C334]
35	RC-SZ1071RC1A-	AK		C	Capacitor (10WV 100μF) [C19,29,916]
36	RCiLZ1002YCZZ-	AG	N	C	Coil (ZJYS51R5-2P) [L103]
37	RCiLZ1028ACZZ-	AH	N	C	Coil (CDRH125-22uH) [L1,101]
38	RCiLZ1056YCZZ	AH		C	Coil (CLS62 100uH) [L3]
39	RCiLZ2038HCZZ-	AH	N	C	Coil (CDRH125-10uH) [L2]
40	RCORF1005YCZZ	AE		C	Core (ACM4532-801) [L801]
41	RCORF1005YCZZ	AE		C	Core (ACM4532-801) [L301,601,602]
42	RCORF1013ACZZ-	AC	N	C	Core (BLM41P600S) [L104]
43	RCORF1024ACZZ-	AC	N	C	Core (BLM21P300S) [L4]
44	RCORF1039ACZZ-	AH		C	Core (AB323SM) [L102]
45	RCRSC1016YCZZ-	AG	N	B	Crystal (32.768kHz) [X201]
46	RCRSC1018YCZZ-	AM	N	B	Crystal (8.064MHz) [X203]
47	RFiLZ1001YCZZ-	AE	N	C	Filter (ACF321825-221) [L622,623,620]
48	RFiLZ1002YCZZ-	AE	N	C	Filter (ACF321825-151) [L604,603,615,616,613,614,619,621,617]
	RFiLZ1002YCZZ-	AE	N	C	Filter (ACF321825-151) [L618,607,608,605,606,609,611,612,610]
49	RFiLZ1029LCZZ-	AE	N	C	Filter (EXCCET101) [L303]
50	RFiLZ1030LCZZ-	AE	N	C	Filter (EXCCET102) [L105]
51	RLMPE1002PCZZ	AG		B	Lamp (DSS-401M) (except PV-500A)
52	RMPTW2220QCJJ	AA		B	Block resistor (22Ω×2) [BR201,206,505]
	RMPTW2220QCJJ	AA		B	Block resistor (22Ω×2) [BR618,619]
53	RMPTW2223QCJJ	AA	N	B	Block resistor (22kΩ×2) [BR606]
54	RMPTW2474QCJJ-	AA	N	B	Block resistor (470kΩ×2) [BR701,302,207,208]
	RMPTW2474QCJJ-	AA	N	B	Block resistor (470kΩ×2) [BR620]
55	RMPTW4000QCJJ-	AA	N	B	Block resistor (0Ω×4) [BR203,215,205,202,204,211,212,213,208,217,216]
56	RMPTW4102QCJJ-	AA	N	B	Block resistor (1kΩ×4) [BR610,609]
57	RMPTW4202QCJJ-	AA	N	B	Block resistor (2kΩ×4) [BR607,608]
58	RMPTW4220QCJJ-	AA	N	B	Block resistor (22Ω×4) [BR506,214]
	RMPTW4220QCJJ-	AA	N	B	Block resistor (22Ω×4) [BR611,612,613,616,601,602,603,604,607,614,615]
59	RMPTW4223QCJJ-	AA	N	B	Block resistor (22kΩ×4) [BR502,501,504,503]
	RMPTW4223QCJJ-	AA	N	B	Block resistor (22kΩ×4) [BR605]
60	RMPTW4474QCJJ-	AA	N	B	Block resistor (470kΩ×4) [BR209,210,301,303]
	RMPTW4474QCJJ-	AA	N	B	Block resistor (470kΩ×4) [BR602,621,901]
⚠ 61	RTRNZ1013ACZZ-	AS	N	B	Transformer (ETJ08Y1AZ) (except PV-500A)[T301]
62	RUNT-1005YCZZ	AU		E	I/R unit [IR801]
63	VCCCCY1HH100D	AA		C	Capacitor (50WV 10PF) [C232,231]
64	VCCCCY1HH180J	AA		C	Capacitor (50WV 18PF) [C205]
65	VCCCCY1HH240J	AA		C	Capacitor (50WV 24pF) [C203]
66	VCCCCY1HH270J	AA		C	Capacitor (50WV 27PF) [C201,202]

5 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
66	VCCCCY1HH270J	AA		C	Capacitor (50WV 27PF)	[C602,604]
67	VCCCCY1HH470J-	AA	N	C	Capacitor (50WV 47PF)	[C109]
68	VCCUCY1AJ105Z	AC		C	Capacitor (10WV 1μF)	[C701,209,210,220,221,222,223,224]
	VCCUCY1AJ105Z	AC		C	Capacitor (10WV 1μF)	[C225,226,227,228,229,230,237]
69	VCKYCY1CB333K	AB		C	Capacitor (16WV 0.033μF)	[C214]
70	VCKYCY1EF103Z-	AA	N	C	Capacitor (25WV 0.010μF)	[C703]
	VCKYCY1EF103Z-	AA	N	C	Capacitor (25WV 0.010μF)	[C702,704,708,709,707,705,706,2,1,22]
71	VCKYCY1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C403,710,501,711,401,812,610,502]
	VCKYCY1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C405,402,404,311,917,26,305,307,306,910,909]
	VCKYCY1EF104Z	AA		C	Capacitor (25WV 0.10μF)	[C607,608,601,309,308,310,7,20,8]
72	VCKYCY1HB102K	AA		C	Capacitor (50WV 1000PF)	[C208,113,112,]
	VCKYCY1HB102K	AA		C	Capacitor (50WV 1000PF)	[C313,314,316,315]
73	VCKYCY1HB103K	AA		C	Capacitor (50WV 0.010μF)	[C213]
74	VCKYCY1HB221K-	AA	N	C	Capacitor (50WV 220PF)	[C107]
75	VCKYCY1HB222K	AA		C	Capacitor (50WV 2200PF)	(except PV-5000A)[C27,28,6,23,332]
	VCKYCY1HB222K	AA		C	Capacitor (50WV 2200PF)	(PV-5000A)[C27,28,6,23]
76	VCKYTL1VF106Z-	AF	N	C	Capacitor (GMK325)(35WV 10μF)	[C103]
77	VCKYTQ1HF334Z-	AC	N	C	Capacitor (50WV 0.33μF)	[C913,104]
78	VCKYTV1CF474Z-	AB	N	C	Capacitor (16WV 0.47μF)	[C108]
79	VCKYTV1HB223K	AA		C	Capacitor (50WV 0.022μF)(223K)	(except PV-5000A)[C331,302]
80	VCTZZA0JD157M	AN		C	Capacitor (6.3WV 150μF)	[C10]
81	VHD1SS355//-1	AB		B	Diode (1SS355)	[D102,8,901,9,7]
82	VHDDAN202U/-1	AB		B	Diode (DAN202U)	[D501,908]
	VHDDAN202U/-1	AB		B	Diode (DAN202U)	[D907]
83	VHDDAP202U/-1	AB		B	Diode (DAP202U)	[D10]
84	VHDEC21QS06-1-	AE		B	Diode (EC21QS06)	[D105]
85	VHDF1AJ3///-1	AE		B	Diode (F1AJ3TP)	[D5,6]
86	VHDNSF03A20-1-	AE		B	Diode (NSF03A20)	[D106]
87	VHDRB050L40-1-	AG	N	B	Diode (RB050L-40)	[D101,104]
88	VHDRB051L40-1-	AE		B	Diode (RB051L-40)	[D103]
89	VHDRB551V30-1-	AD	N	B	Diode (RB551V-30)	[D1,3,4,12]
90	VHDS1ZB60//-1	AC		B	Diode (S1ZB60)	(except PV-5000A)[DB301]
91	VHERD33P///-1-	AE	N	B	Zener diode (RD33P)	(except PV-5000A)[DZ301]
92	VHERLZ27B//-1-	AC	N	B	Zener diode (RLZ27B)	[D107]
93	VHERLZ3.6A/-1-	AC	N	B	Zener diode (RLZ3.6A)	(except PV-5000A)[DZ305,304]
94	VHERLZ51///-1	AB		B	Zener diode (RLZ51)	(except PV-5000A)[DZ303,302]
95	VHHRXE017//-1	AF		B	Thermistor (RXE017)	(except PV-500A)
96	VHi165165TS50	BH	N	B	IC (64M DRAM)(165165TS50)	(U.S.A)[IC402,401]
	VHi165165TS50	BH	N	B	IC (64M DRAM)(165165TS50)	(except U.S.A)[IC404,402,401,403]
97	VHi16V104CTL5	BA	N	B	IC (KM416V1004CT-5)	[IC602]
98	VHi74LCX244FT	AH		B	IC (TC74LCX244)	[IC603]
99	VHiLT1511//-1	BA		B	IC (LT1511)	[IC101]
100	VHiNJM2135V-1-	AG	N	B	IC (NJM2135V)	[IC304]
101	VHiRN5VD20A-1-	AA	N	B	IC (RN5VD20A)	[IC203]
102	VHiS80855ANNP-	AD	N	B	IC (S80855ANNP)	[IC904]
103	VHiS80920ANMP-	AE	N	B	IC (S80920AN)	[IC202]
104	VHiS816A27AMC-	AE	N	B	IC (S816A27AMC)	[IC6]
105	VHiS816A33AMC-	AE	N	B	IC (S816A33AMC)	[IC5]
106	VHiSB2020P372-	AL	N	B	IC (SB2020P)	[IC2]
107	VHiSB3052P/-1-	AW	N	B	IC (SB3052P)	[IC1]
108	VHiSC123070J1	AS	N	B	IC (SC12307-0J)	[IC501]
109	VHiSED1354/-1	BC	N	B	IC (SED1354)	[IC601]
110	VHiTC35143AF1	BA	N	B	IC (TC35143AF)	[IC301]
111	VHiTC58FVB4FT	AY	N	B	IC (TC58FVT400-85)	[IC405]
112	VHiTC6345AFGA	AZ		B	IC (TC6345AF)	[IC701]
113	VHiTC7S66U/-1-	AF	N	B	IC (TC7S66U)	[IC305]
114	VHiTC7SH00FU1-	AD	N	B	IC (TC7SH00FU)	[IC3]
115	VHiTC7SH08FU1	AE		B	IC (TC7SH08FU)	[IC702]
	VHiTC7SH08FU1	AE		B	IC (TC7SH08FU)	[IC905,906,907]
116	VHiTC7W08FU-1	AE		B	IC (TC7W08FU)	[IC902]
117	VHiTPS2211iDB-	AV	N	B	IC (TPS2211)	[IC901]
118	VHiTX3922//-1	BN	N	B	IC (TMPR3922U)	[IC201]
119	VHiUPD4722/-1-	AQ	N	B	IC (UPD4722)	[IC801]
120	VHPGL3KG44/-1	AB		B	LED (GL3KG44)	
121	VHPPC354NT/-1-	AF	N	B	Photo copupler (PC354NT)	(except PV-5000A)[IC303]
122	VHRAQV214S/-1-	AR	N	B	Photomos relay (AQV214S)	(except PV-5000A)[IC302]
123	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)	[R701,232,516,703,201,221,208,316,315,804]
	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)	[R806,805,210,213,803,404,402,802,801]
	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)	[C206]
	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)	[R706,702,902,408,233,901,704,335,904,342]
	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)	(except PV-5000A)[R309,308]
	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)	[R341,102,403,401,340,602,601,903,339,930,224]
	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)	(except PV-5000A)[F301]
	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%)	[D11]
124	VRS-CY1JD100J	AA		C	Resistor (1/16W 10Ω ±5%)	[R327,330,329,328,321]
	VRS-CY1JD100J	AA		C	Resistor (1/16W 10Ω ±5%)	[R2,320,3[illegible]0,336,3]
125	VRS-CY1JD101J	AA		C	Resistor (1/16W 100Ω ±5%)	[R311]
	VRS-CY1JD101J	AA		C	Resistor (1/16W 100Ω ±5%)	[R17,6,13]
126	VRS-CY1JD102J	AA		C	Resistor (1/16W 1.0KΩ ±5%)	[R508]
	VRS-CY1JD102J	AA		C	Resistor (1/16W 1.0KΩ ±5%)	[R130,123,124,129,101,32,927]

PV-5000
PV-5000A

5 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
126	VRS-CY1JD102J	AA		C	Resistor (1/16W 1.0KΩ ±5%)	[R22,24,23,911,615,931,120]
127	VRS-CY1JD103J	AA		C	Resistor (1/16W 10KΩ ±5%)	[R337,314]
	VRS-CY1JD103J	AA		C	Resistor (1/16W 10KΩ ±5%)	[R115,212,313,128,114,715]
128	VRS-CY1JD104F	AA		C	Resistor (1/16W 100KΩ ±1%)	[R26]
129	VRS-CY1JD104J	AA		C	Resistor (1/16W 100KΩ ±5%)	[R711,318,514,515,236,241]
	VRS-CY1JD104J	AA		C	Resistor (1/16W 100KΩ ±5%)	[R215,25,714,712,209,713,909,134,720,709,708,707,119,710]
	VRS-CY1JD104J	AA		C	Resistor (1/16W 100KΩ ±5%)	(except PV-5000A)[R237]
	VRS-CY1JD104J	AA		C	Resistor (1/16W 100KΩ ±5%)	(PV-5000A)[R236]
130	VRS-CY1JD105J	AA		C	Resistor (1/16W 1MΩ ±5%)	[R507]
	VRS-CY1JD105J	AA		C	Resistor (1/16W 1MΩ ±5%)	[R405,205,928]
131	VRS-CY1JD124J-	AA	N	C	Resistor (1/16W 120KΩ ±5%)	[R121]
132	VRS-CY1JD151F	AA		C	Resistor (1/16W 150Ω ±1%)	[R509]
	VRS-CY1JD151F	AA		C	Resistor (1/16W 150Ω ±1%)	(except PV-5000A)[R307,306]
133	VRS-CY1JD152J-	AA	N	C	Resistor (1/16W 1.5KΩ ±5%)	[R331,326,338]
134	VRS-CY1JD153F-	AA	N	C	Resistor (1/16W 15KΩ ±1%)	(except PV-5000A)[R332]
135	VRS-CY1JD154F	AA		C	Resistor (1/16W 150KΩ ±1%)	(except PV-5000A)[R29]
136	VRS-CY1JD183J	AA		C	Resistor (1/16W 18KΩ ±5%)	[R302]
137	VRS-CY1JD184F	AA		C	Resistor (1/16W 180kΩ ±1%)	[R27]
138	VRS-CY1JD204F	AA		C	Resistor (1/16W 200kΩ ±1%)	[R28]
139	VRS-CY1JD220J-	AA	N	C	Resistor (1/16W 22Ω ±5%)	[R216,219,239,217,218,220]
	VRS-CY1JD220J-	AA	N	C	Resistor (1/16W 22Ω ±5%)	[R614,611,612,613,238]
140	VRS-CY1JD223J-	AA	N	C	Resistor (1/16W 22KΩ ±5%)	[R618]
141	VRS-CY1JD271J-	AA	N	C	Resistor (1/16W 270Ω ±5%)	[R106]
142	VRS-CY1JD333J-	AA	N	C	Resistor (1/16W 33KΩ ±5%)	[R907,20]
143	VRS-CY1JD334J	AA		C	Resistor (1/16W 330KΩ ±5%)	[R202]
144	VRS-CY1JD361J	AA		C	Resistor (1/16W 360Ω ±5%)	(except PV-5000A)[R305]
145	VRS-CY1JD363F-	AA	N	C	Resistor (1/16W 36kΩ ±1%)	[R323]
146	VRS-CY1JD391J	AA		C	Resistor (1/16W 390Ω ±5%)	[R5]
147	VRS-CY1JD472J	AA		C	Resistor (1/16W 4.7KΩ ±5%)	[R222]
148	VRS-CY1JD473J	AA		C	Resistor (1/16W 47KΩ ±5%)	[R716]
	VRS-CY1JD473J	AA		C	Resistor (1/16W 47KΩ ±5%)	[R920,919,14,18,30]
149	VRS-CY1JD474J-	AA	N	C	Resistor (1/16W 470KΩ ±5%)	[R717,718,322,504,503,506,325,505,501]
	VRS-CY1JD474J-	AA	N	C	Resistor (1/16W 470KΩ ±5%)	[R813,206,812,227,207,811,228,230,229]
	VRS-CY1JD474J-	AA	N	C	Resistor (1/16W 470KΩ ±5%)	[R617,616,126,12,16,4,15,125,511]
	VRS-CY1JD474J-	AA	N	C	Resistor (1/16W 470KΩ ±5%)	[R31,19,510,11,240,211,513,908,512]
150	VRS-CY1JD511J-	AA	N	C	Resistor (1/16W 510Ω ±5%)	[R104]
151	VRS-CY1JD823J-	AA	N	C	Resistor (1/16W 82KΩ ±5%)	[R906]
152	VRS-CY1JS201D-	AA	N	C	Resistor (1/16W 200Ω±0.5%)	[R109,108]
153	VRS-CY1JS512D-	AA	N	C	Resistor (1/16W 5.1KΩ±0.5%)	[R107]
154	VRS-TD3AD100J-	AC		C	Resistor (1W 10Ω ±5%)	[R810]
155	VRS-TD3AD101J	AC		C	Resistor (1W 100Ω ±5%)	[R1]
156	VRS-TD3AD470J-	AC	N	C	Resistor (1W 47Ω ±5%)	(except PV-5000A)[R333,303]
157	VRS-TE2HFR10F	AC	N	C	Resistor (1/2W 0.1Ω ±1%)	[R105,110]
158	VRS-TS2AD000J-	AA		C	Resistor (1/10W 0Ω ±5%)	[R131,36]
	VRS-TS2AD000J-	AA		C	Resistor (1/10W 0Ω ±5%)	[F302,902,6,3,2,1,9,5,4]
159	VRS-TS2AD100J	AA		C	Resistor (1/10W 10Ω ±5%)	[R35]
160	VRS-TS2AD221J-	AA		C	Resistor (1/10W 220Ω ±5%)	[R122]
161	VRS-TS2AQ303B-	AC	N	C	Resistor (1/10W 30kΩ ±0.1%)	[R113]
162	VRS-TW2ED101J-	AB	N	C	Resistor (1/4W 100Ω ±5%)	[R808]
163	VRS-TX2HD752J-	AC	N	C	Resistor (1/2W 7.5KΩ ±5%)	(except PV-5000A)[R304]
164	VRSTS2AQ1273B-	AC	N	C	Resistor (1/10W 127kΩ ±0.1%)	[R112]
165	VRSTS2EFR033J-	AC	N	C	Resistor (1/4W 33mΩ ±5%)	[R8,10]
166	VS2SA1213Y/-1	AC		B	Transistor (2SA1213Y)	[Q14,15,16]
167	VS2SD1702//-1-	AE	N	B	Transistor (2SD1702)	(except PV-5000A)[Q301]
168	VS2SJ346///-1-	AC	N	B	Transistor (2SJ346)	[Q503,306]
169	VS2SJ501///-1	AF		B	Transistor (2SJ501)	[Q801]
170	VS2SK1824//-1	AB		B	Transistor (2SK1824)	[Q802,305,501]
	VS2SK1824//-1	AB		B	Transistor (2SK1824)	[Q304,22,106,21,13,107,19,8,7,6,20,12,108]
171	VSDTA114EUA-1-	AC	N	B	Transistor (DTA114EU)	[Q17]
172	VSDTC144EUA-1-	AC	N	B	Transistor (DTC144EU)	[Q502,909,103]
	VSDTC144EUA-1-	AC	N	B	Transistor (DTC144EU)	(except PV-5000A)[Q303]
173	VSMUN5113//-1-	AC	N	B	Transistor (MUN5113)	(except PV-5000A)[Q302]
174	VSNDS356AP/-1-	AF	N	B	Transistor (NDS356AP)	[Q908,9]
175	VSNDS8434A/-1	AL		B	Transistor (NDS8434A)	[Q10,5]
176	VSSi4435DY/-1-	AN	N	B	Transistor (SI4435DY)	[Q11]
177	VSTM3111///-1-	AG	N	B	Transistor (TM3111)	[Q2,3,4,1]
178	XBBSD20P06000	AA		C	Screw (2×6)	
	(Unit)					
901	DUNTK1784YCZZ		N	E	Main PWB unit	[U.S.A]
	DUNTK1738YCZZ		N	E	Main PWB unit	[Canada,Hong Kong]
	DUNTK1752YCZZ		N	E	Main PWB unit	[PV-5000A]

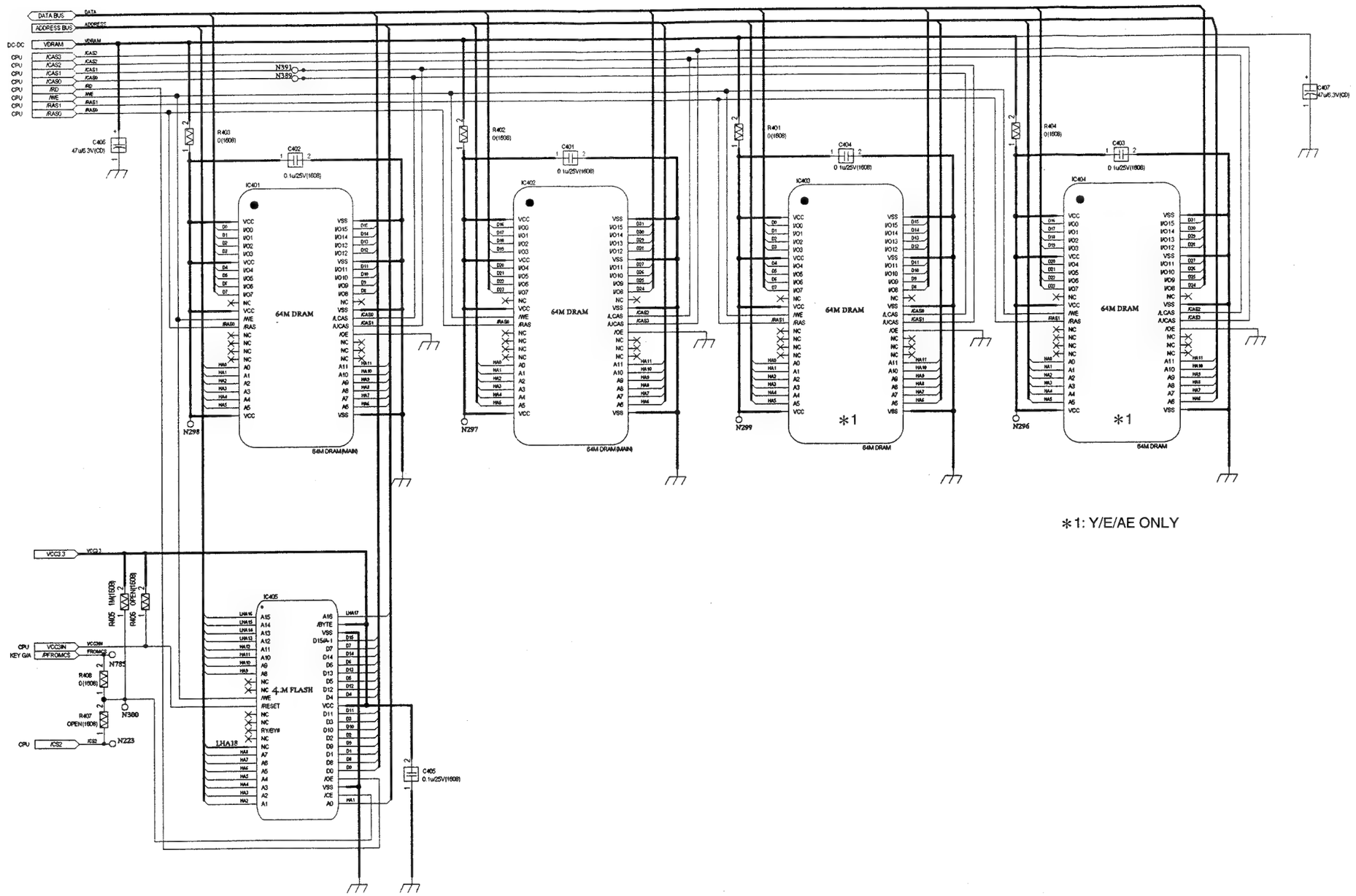
6 Memory PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW1051YC80	AN		C	Connector (80pin) [CN1A]
2	VCKYCY1EF104Z	AA		C	Capacitor (25WV 0.10μF) [C2A,3A,4A]
3	VRS-CY1JD000J	AA		C	Resistor (1/16W 0Ω ±5%) [R2A,4A,5A]
	(Unit)				
901	DUNTK1741YCZZ		N	E	Memeory PWB unit

7 LED sub PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	PSPAZ1108LCZZ	AD		C	LED spacer
2	QCNW-1024YCZZ	AD	N	C	LED cable
3	VHPGL3HS43/-1	AB		B	LED (Orange) (GL3HS43)
	(Unit)				
901	DUNTK1749YCZZ		N	E	LED sub PWB unit

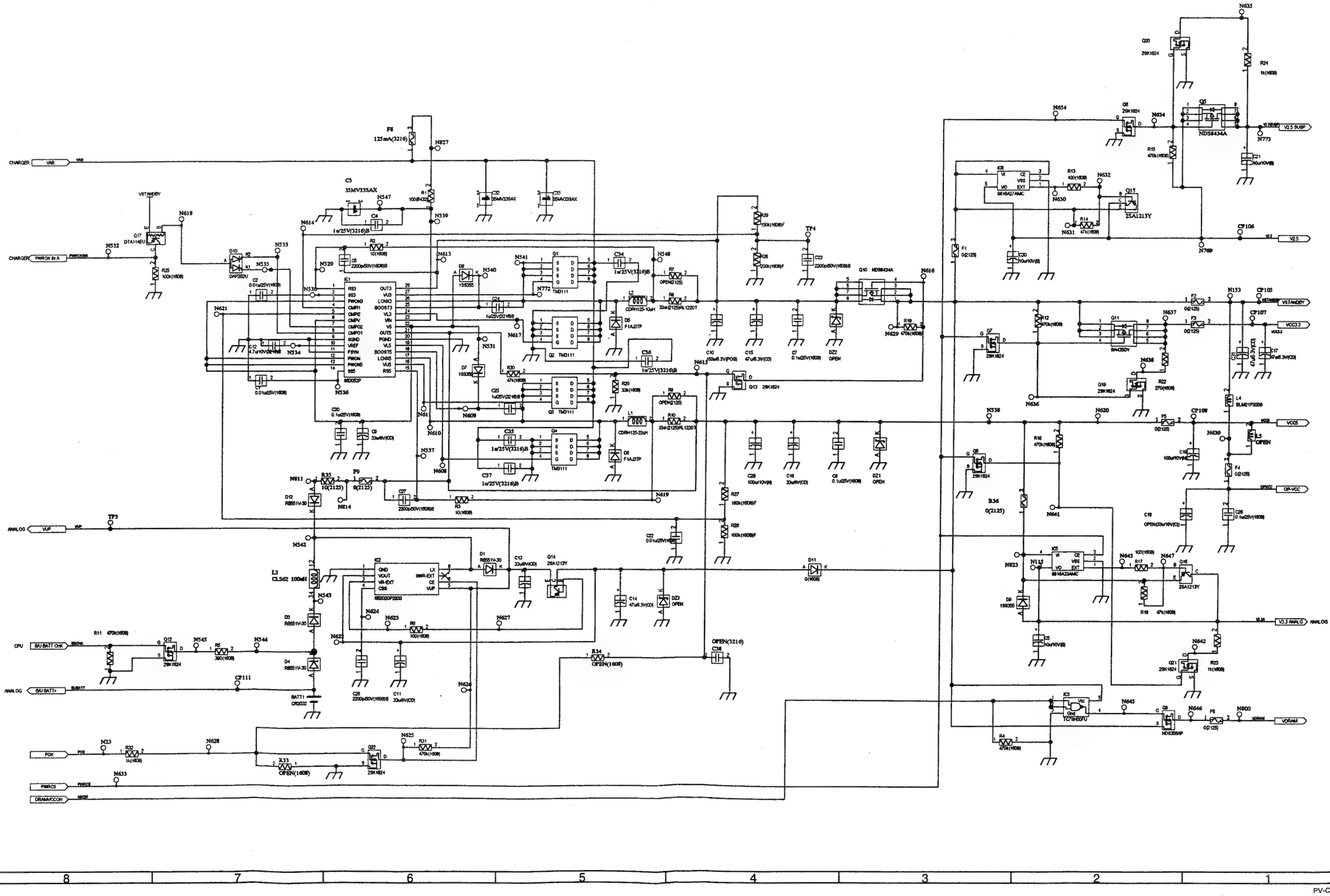
(1) INTERNAL MEMORY



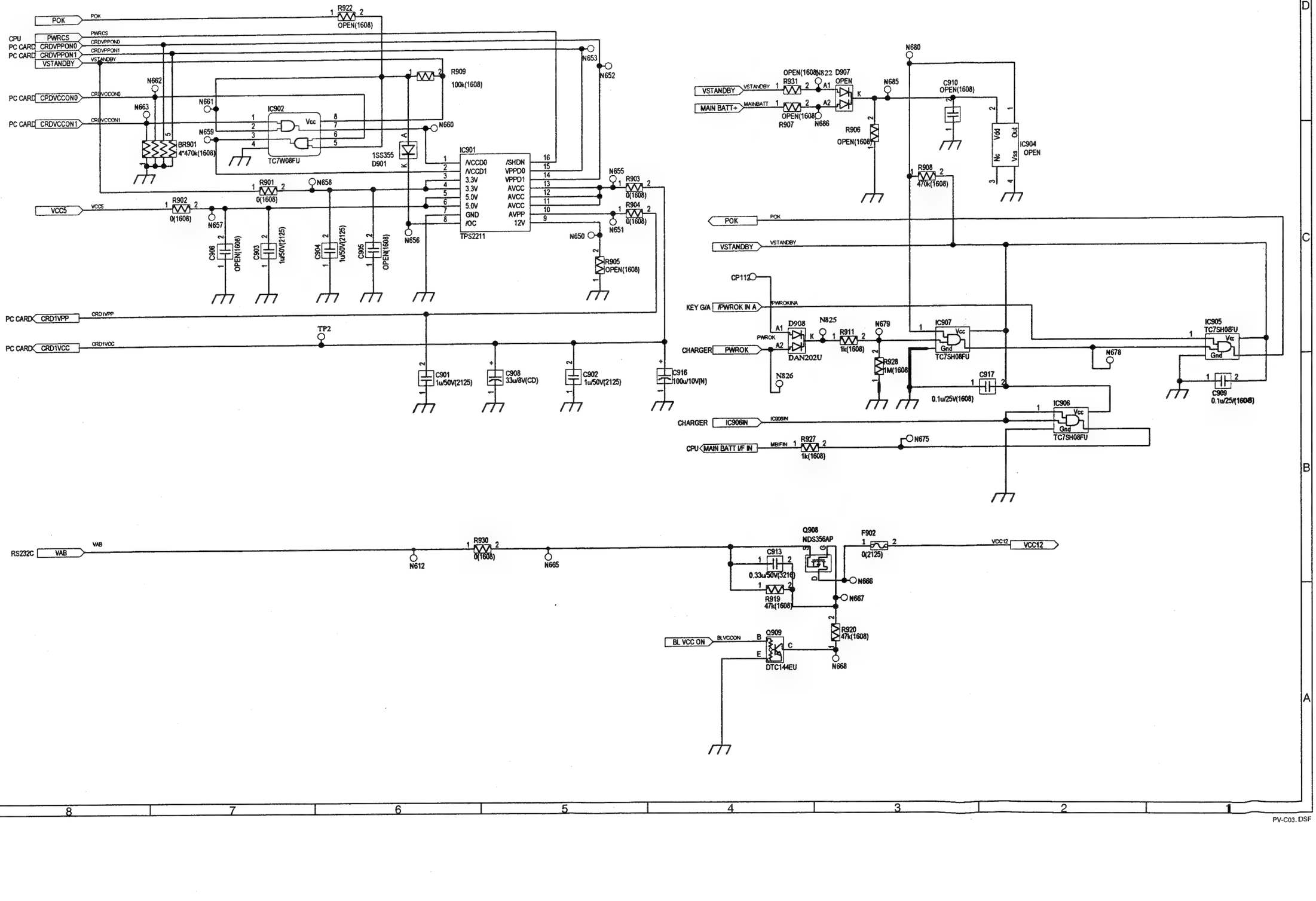
*1: Y/E/AE ONLY

PV-C01.DSF

(2) DC-DC CONVERTER

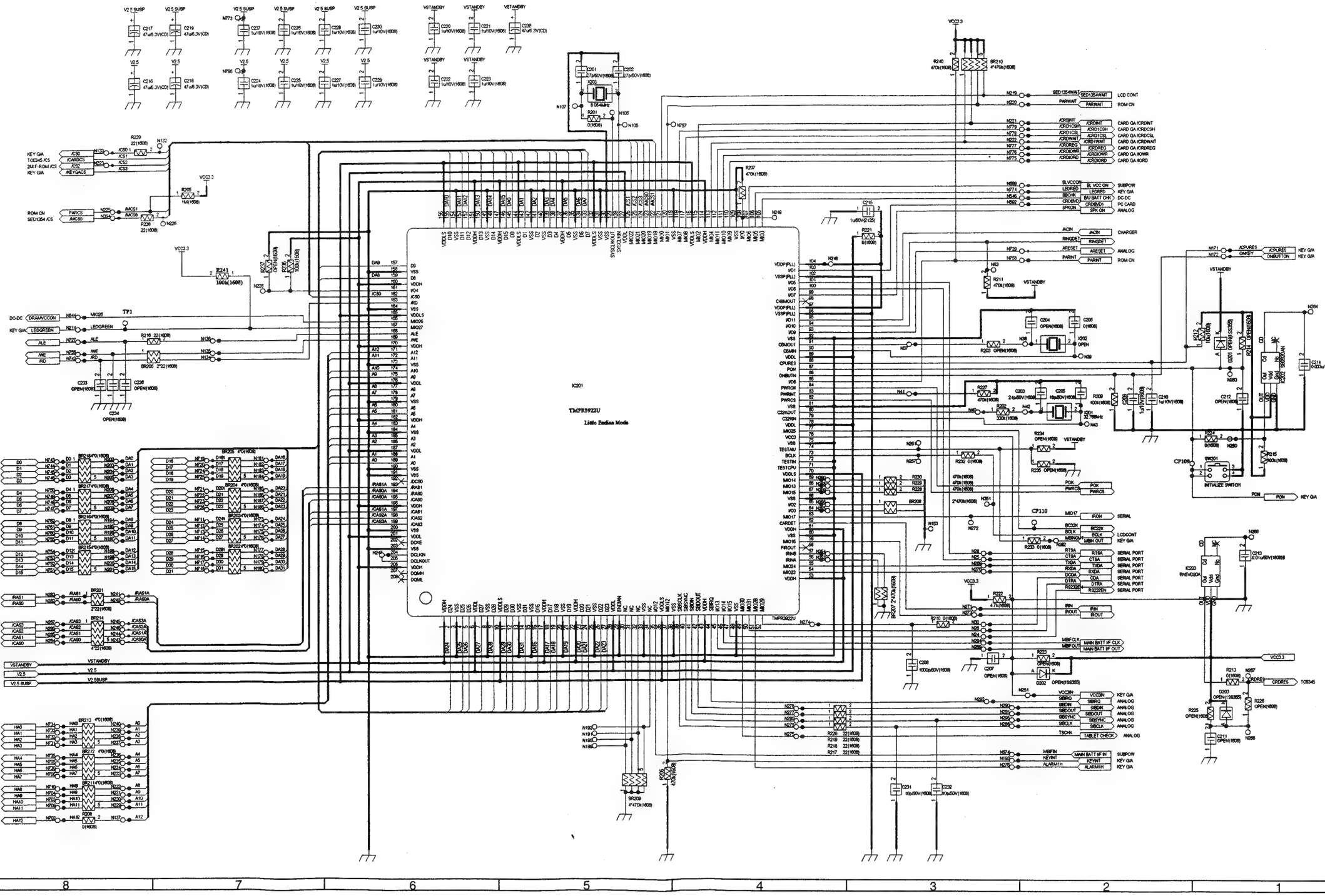


(3) SUB POWER BLOCK



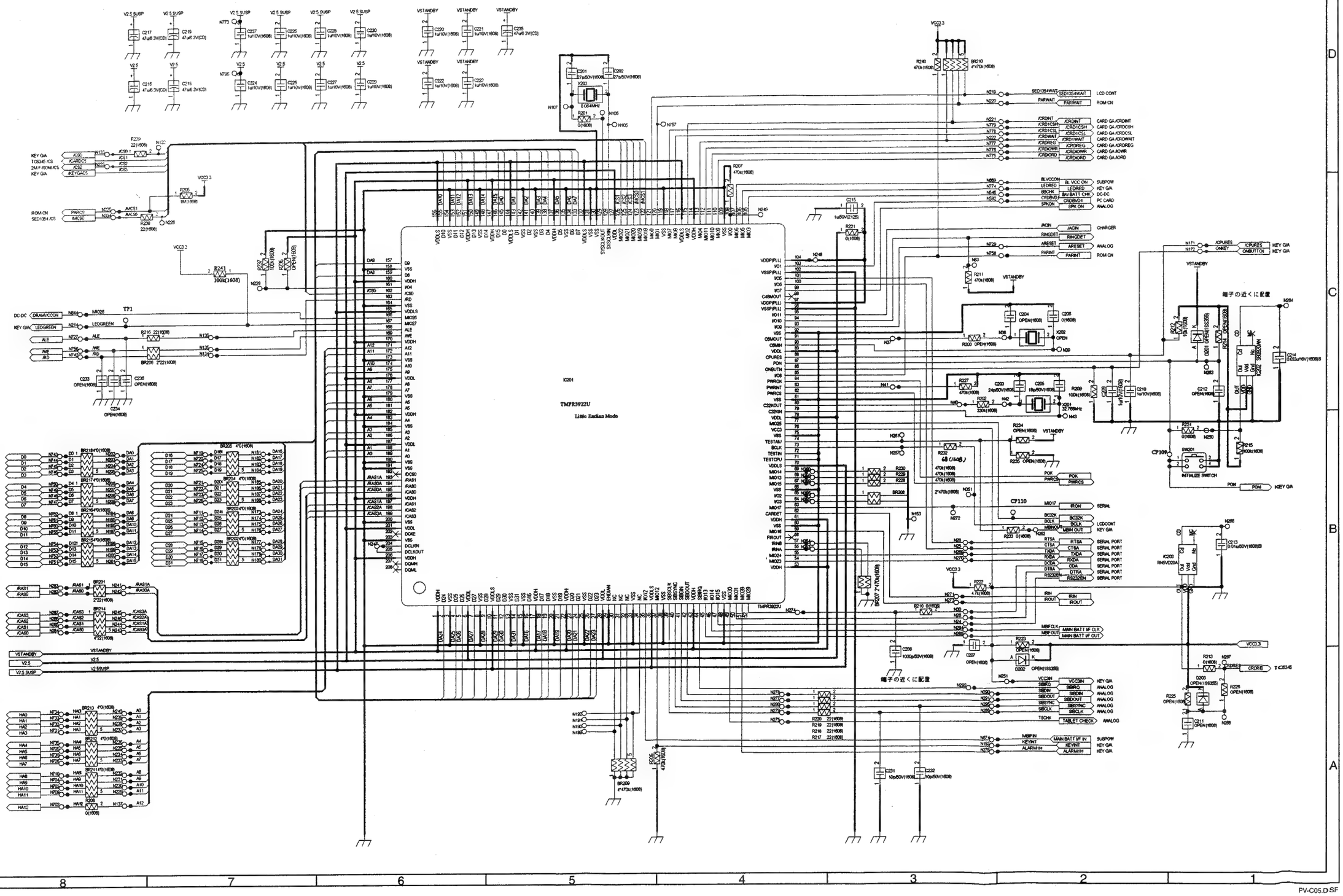
PV-C03.DSF

(4) CPU

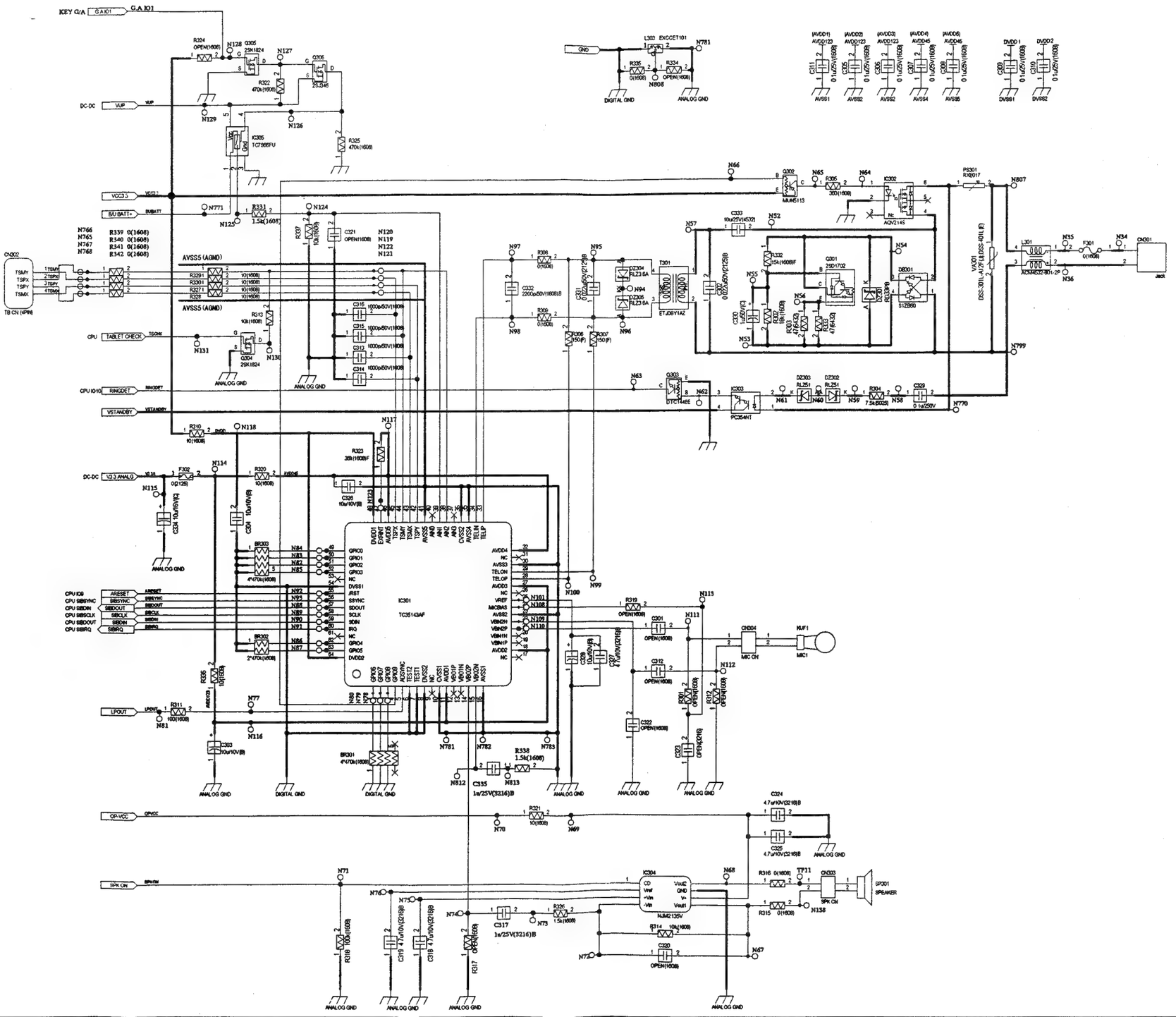


PV-C04.DSF

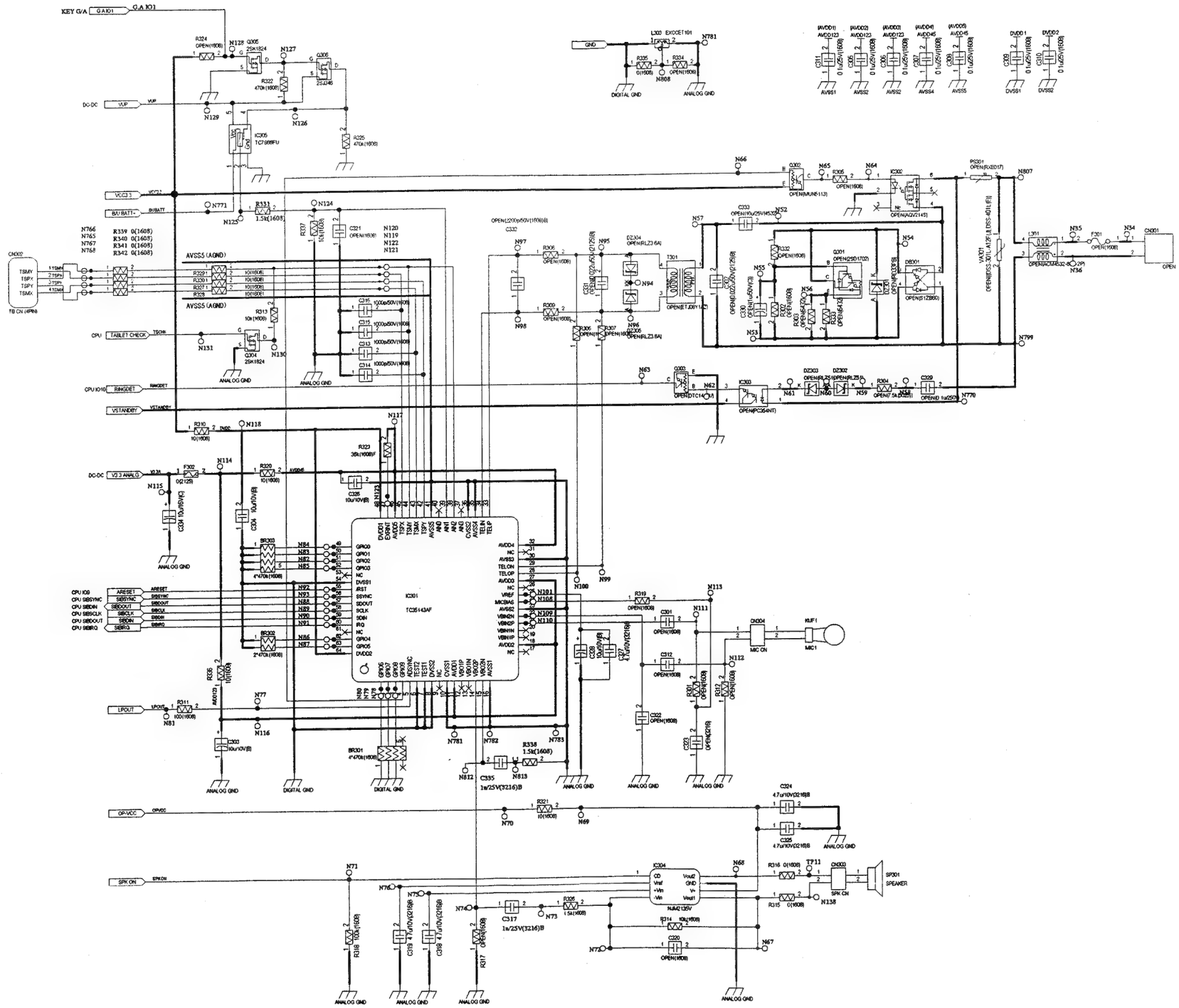
(4) CPU (A version only)



(5) ANALOG LOGIC

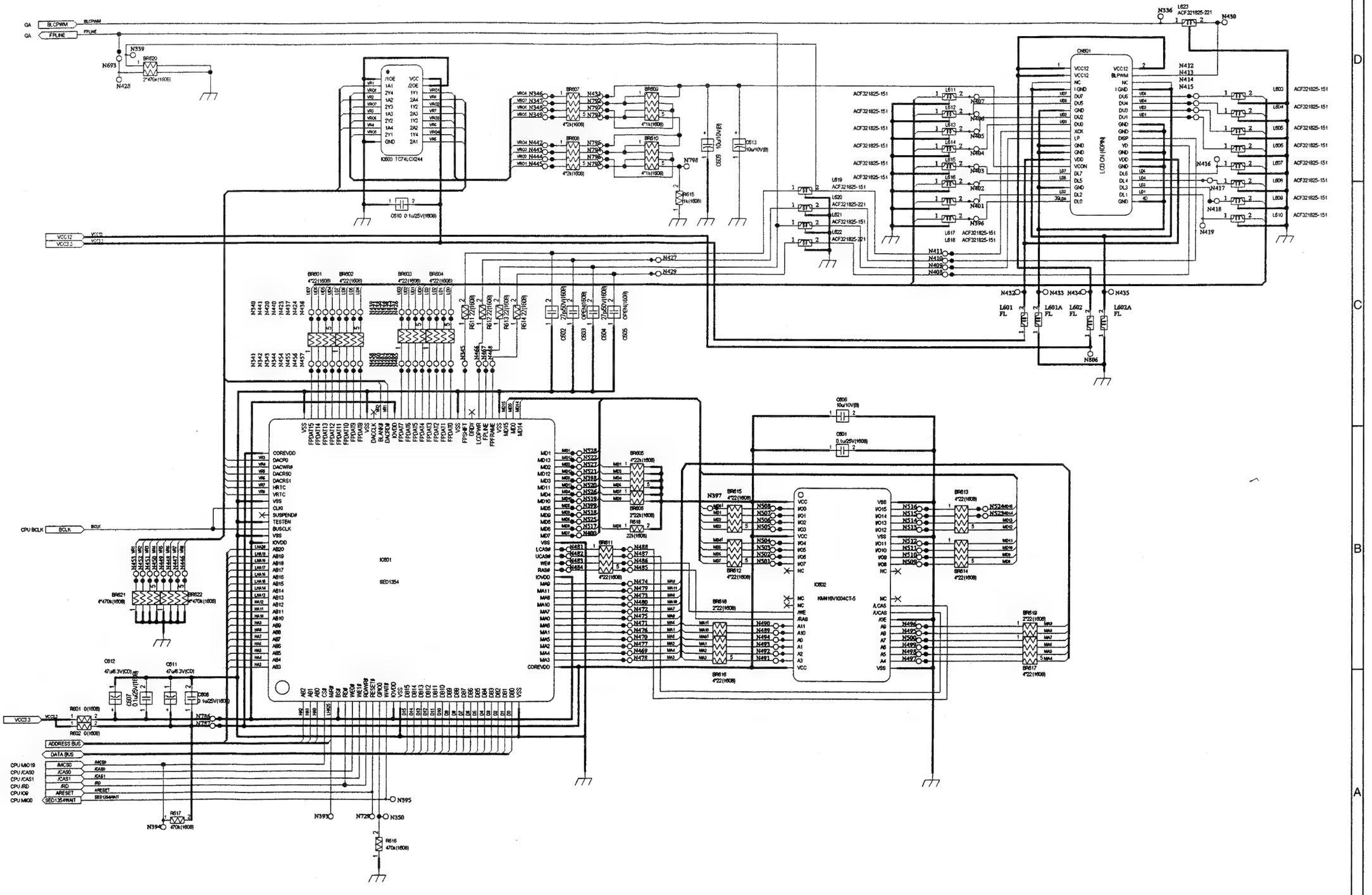


(5) ANALOG LOGIC (A version only)



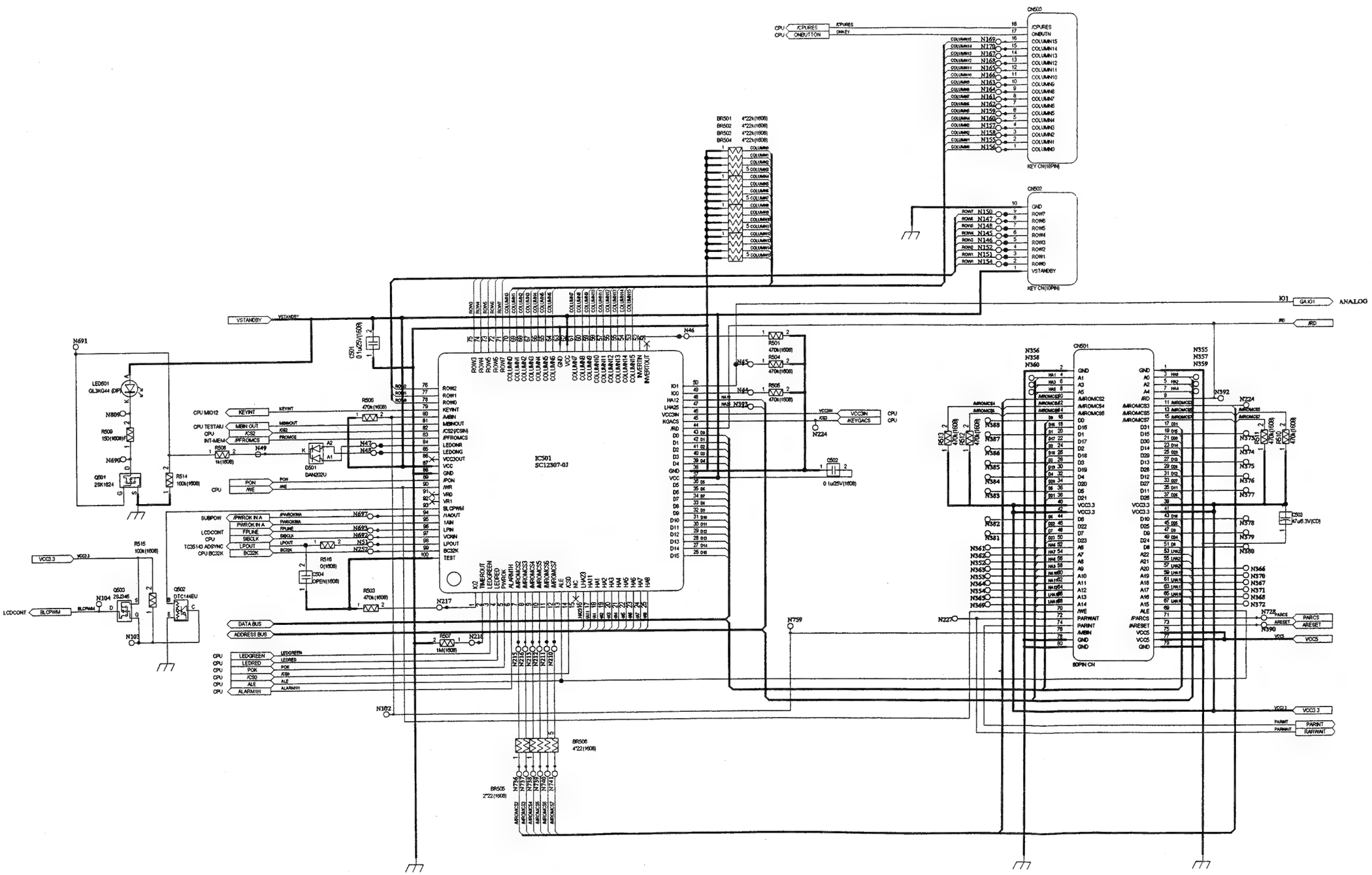
PV-C07.DSF

(6) LCD CONTROLLER



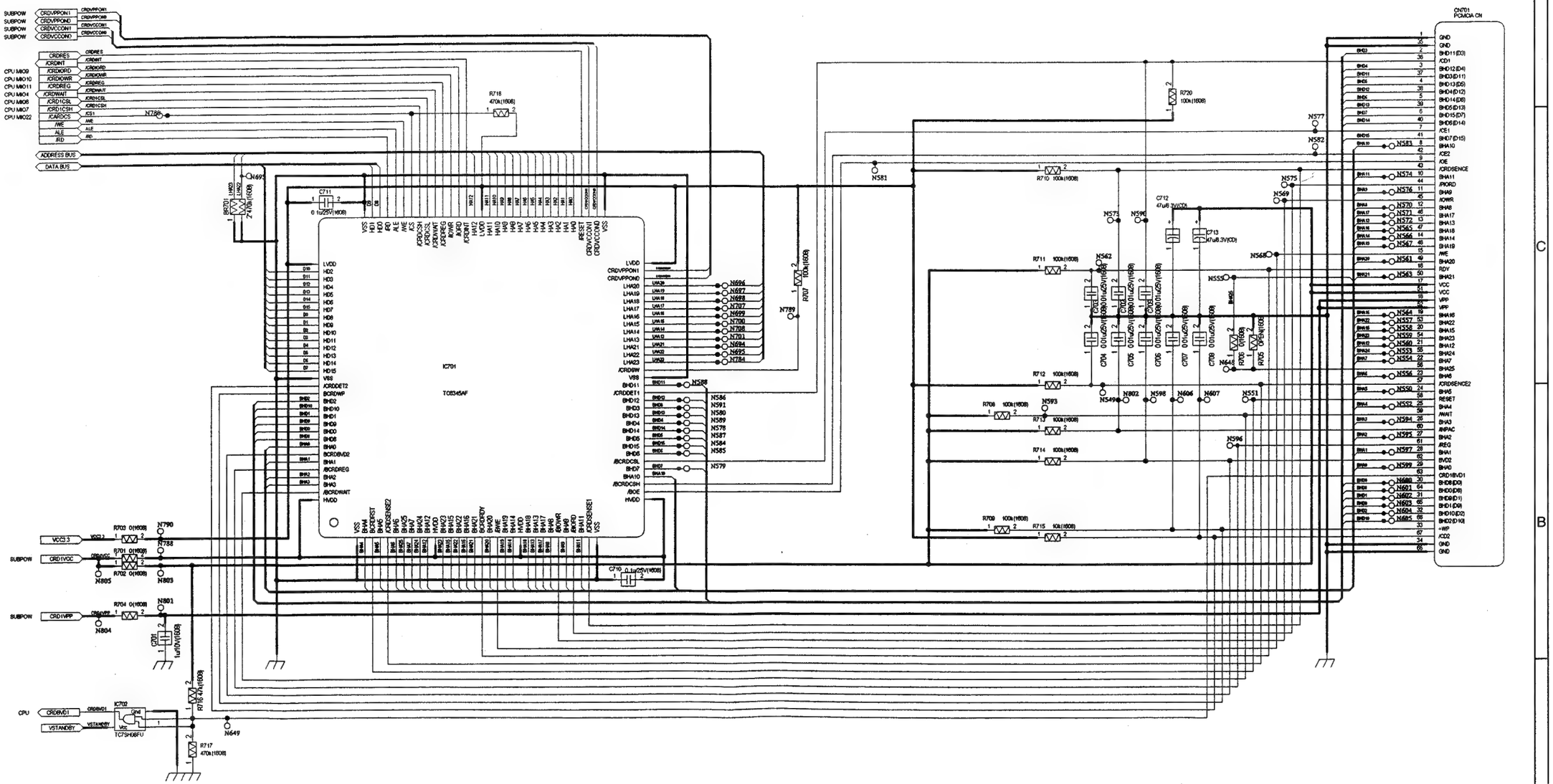
PV-C08.DSF

(7) KEY G/A



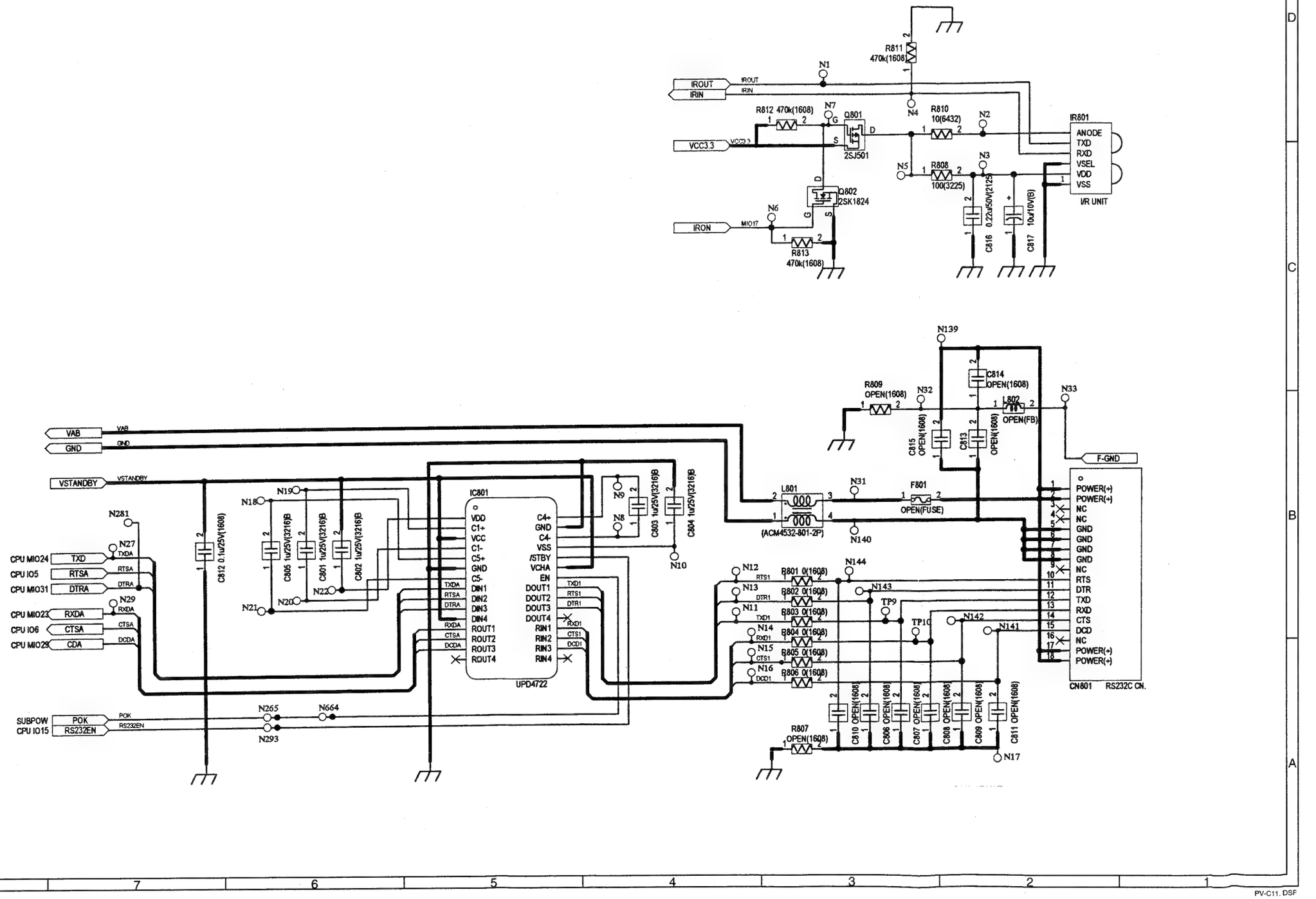
PV-C09.DSF

(8) PCMCIA CARD CONTROLLER



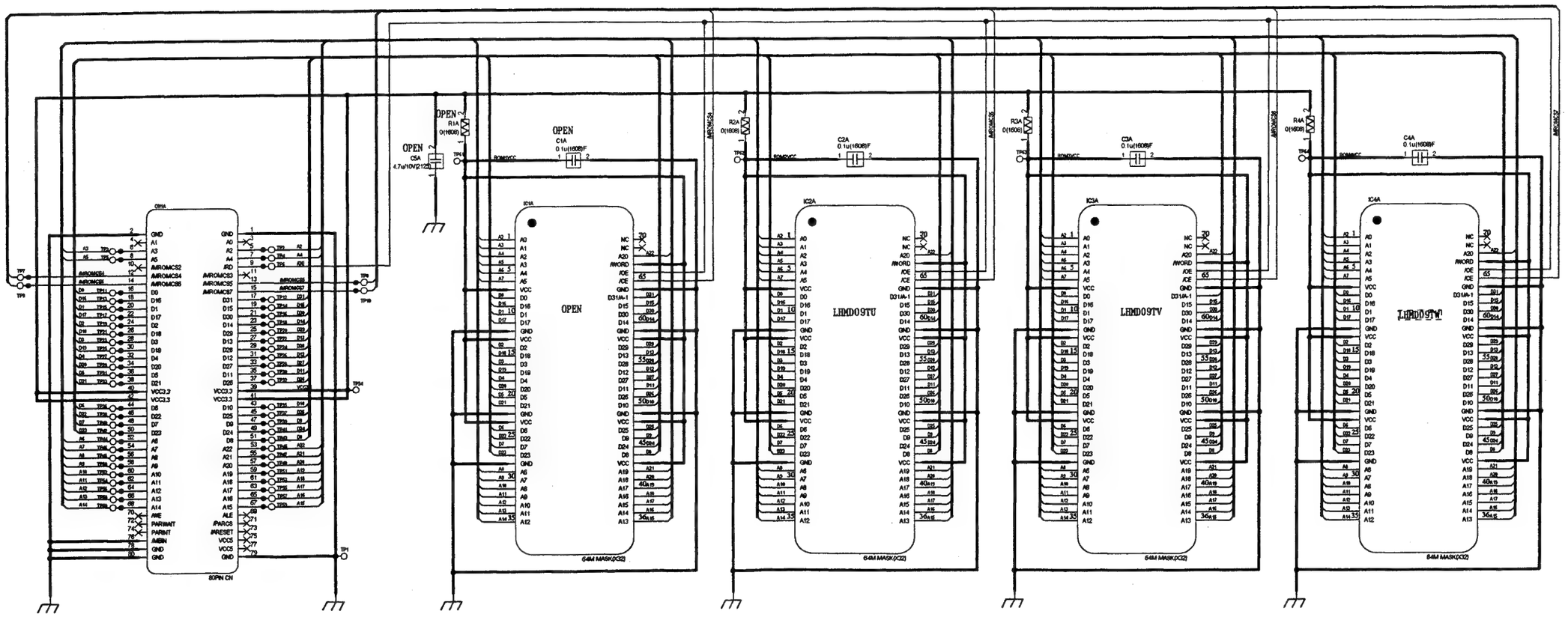
PV-C10.DSF

(9) RS-232C SERIAL PORT / IR PORT



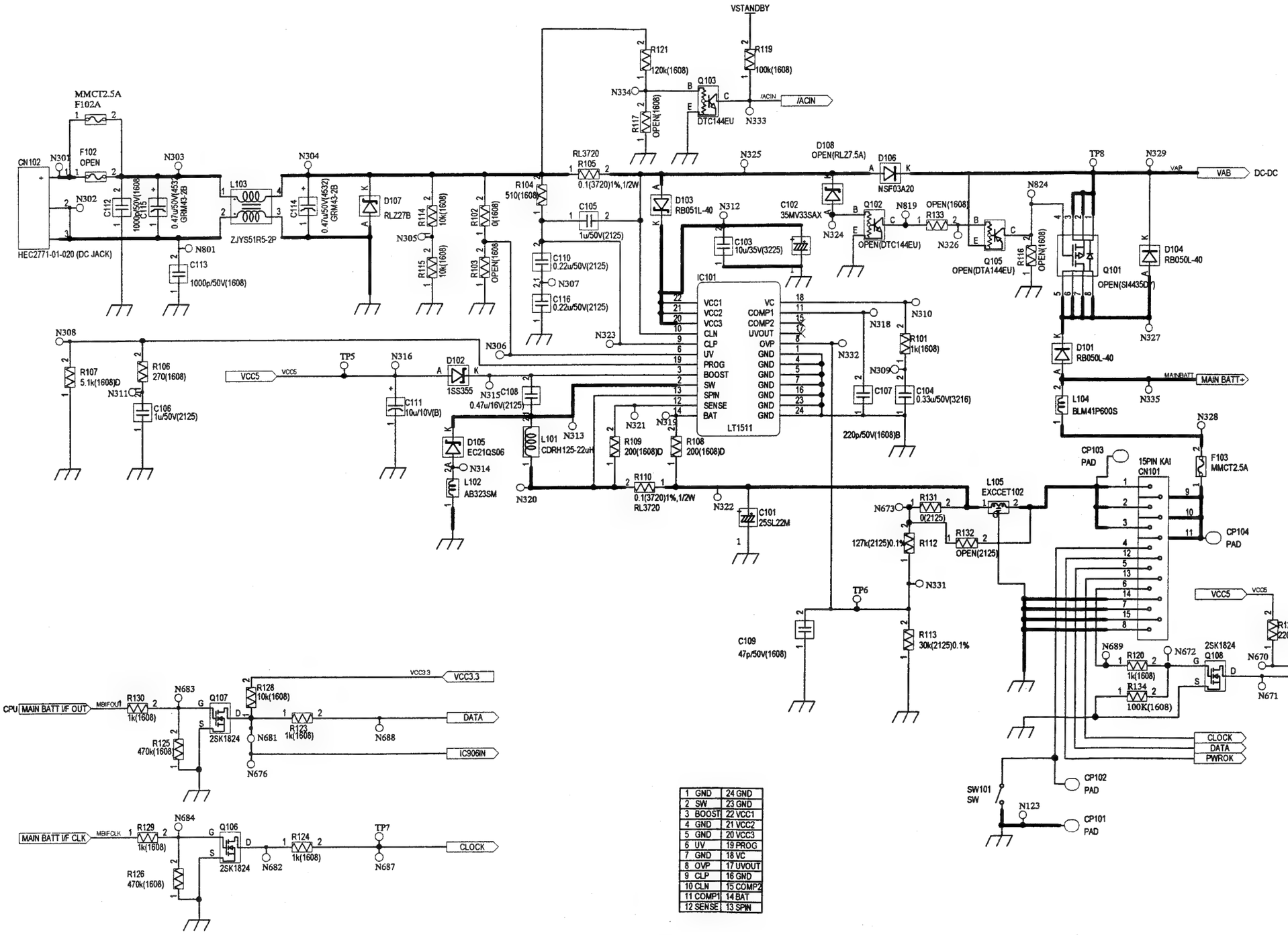
PV-C11. DSF

(10) EXPAND MEMORY MODULE



PV-C12.DSF

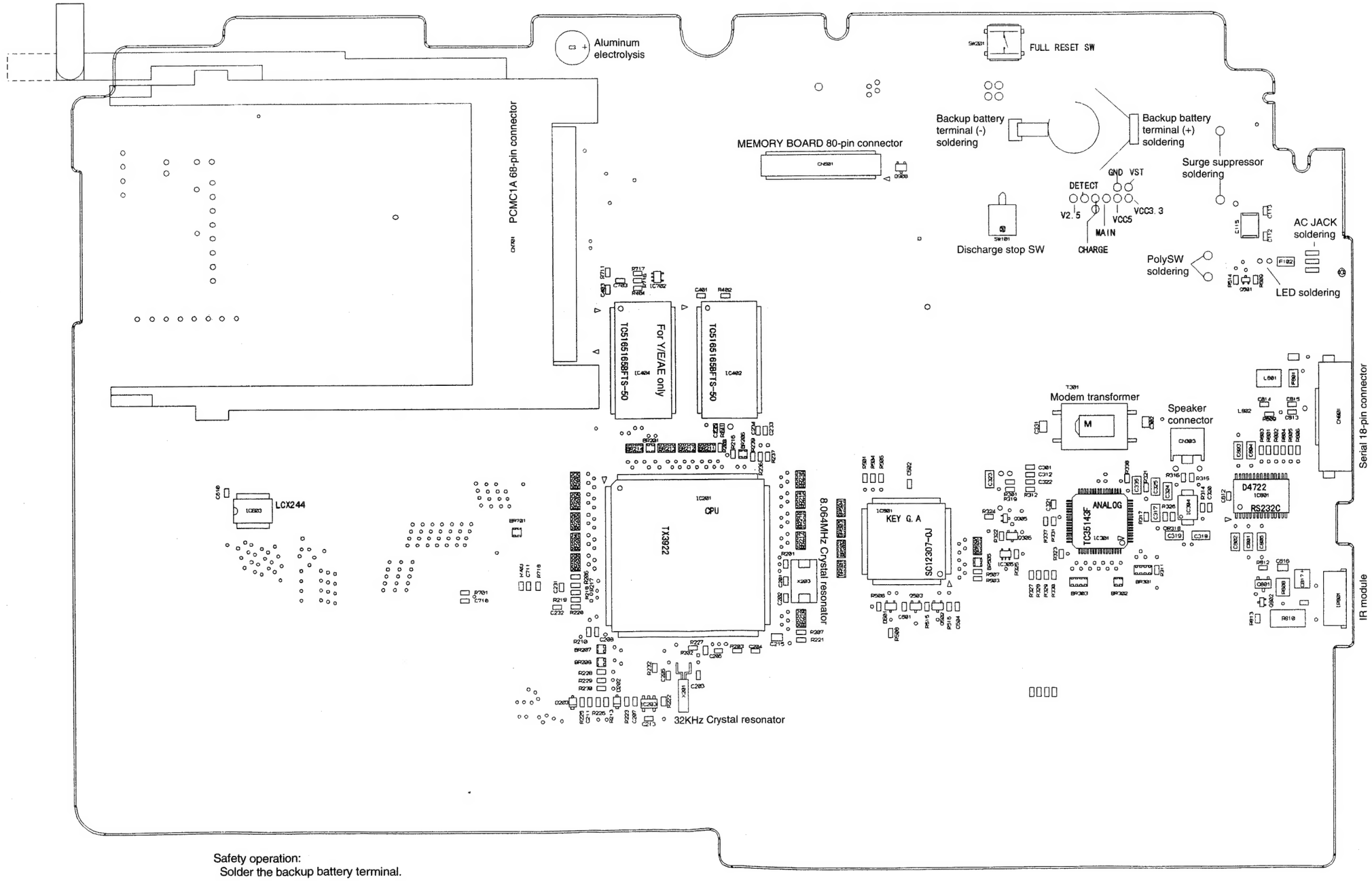
(11) CHARGER



1 GND	24 GND
2 SW	23 GND
3 BOOST	22 VCC1
4 GND	21 VCC2
5 GND	20 VCC3
6 UV	19 PROG
7 GND	18 VC
8 OVP	17 UVOUT
9 CLP	16 GND
10 CLN	15 COMP2
11 COMP1	14 BAT
12 SENSE	13 SPIN

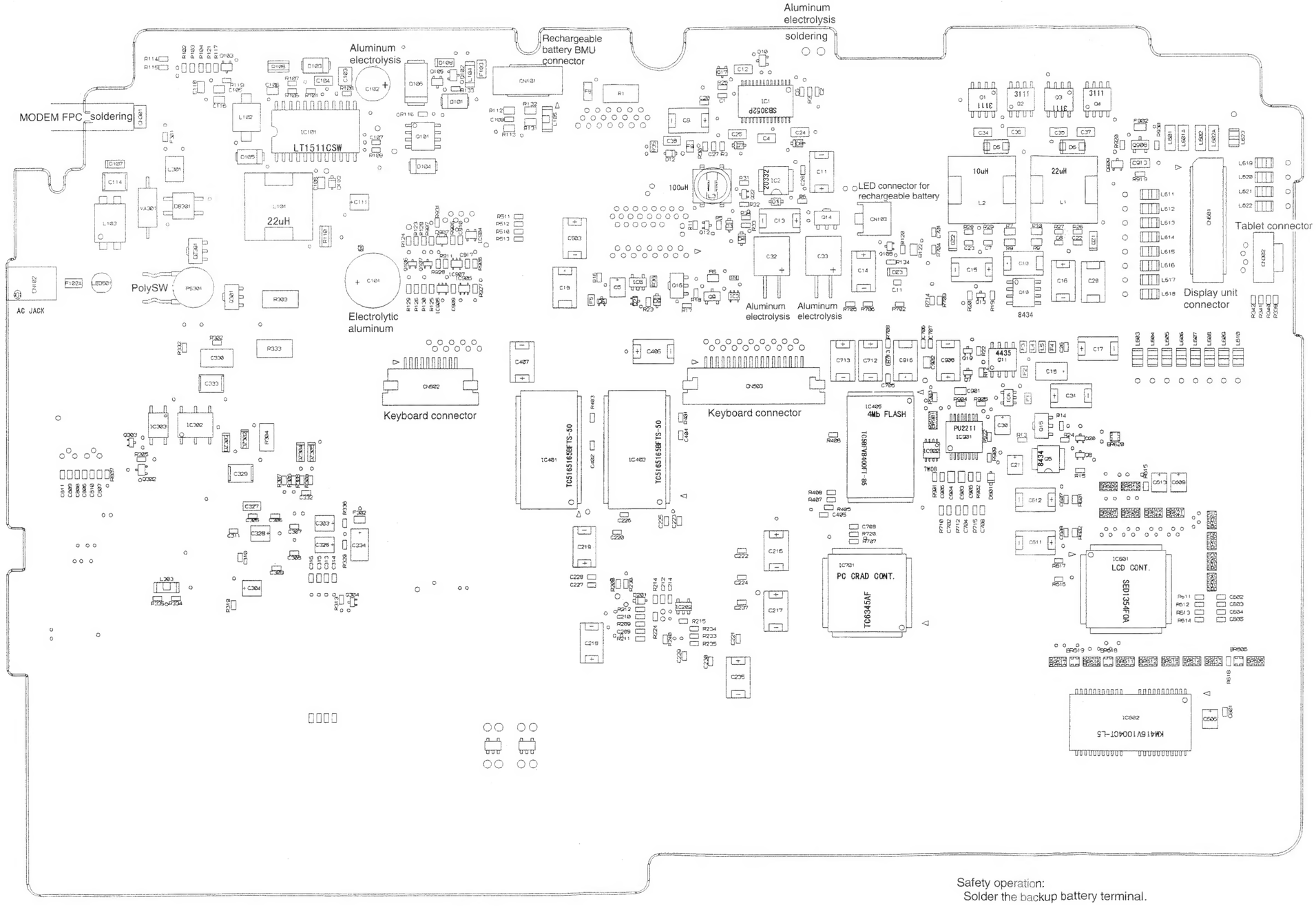
PV-C13.DSF

(12) MAIN PWB PARTS LAYOUT (A side)



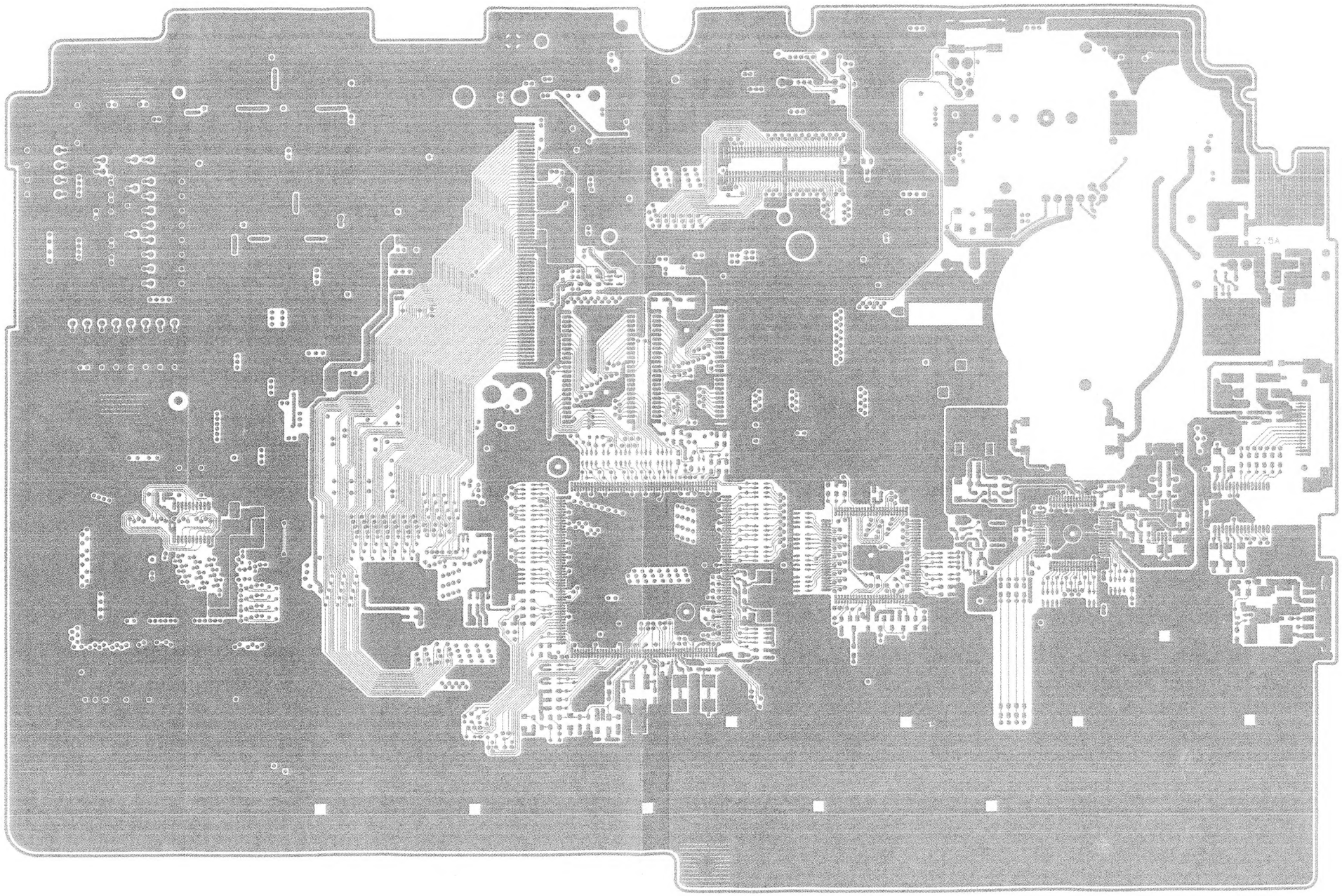
Safety operation:
Solder the backup battery terminal.

(13) MAIN PWB PARTS LAYOUT (B side)



Safety operation:
Solder the backup battery terminal.

(14) MAIN PWB PATTERN (A side)



PV-P03.DSF

(15) MAIN PWB PATTERN (B side)